ARAT TECHNOLOGICAL UNIVERSITY

SEMESTER-VI(NEW) – EXAMINATION – SUMMER 2019 Subject Code:2161101

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Subject Name: VLSI Technology & Design

Total Marks: 70

Time:10:30 AM TO 01:00 PM Instructions:

- 1. Attempt all questions.
- 2. Make suitable assumptions wherever necessary.
- 3. Figures to the right indicate full marks
- 03 **Q.1** (a) Explain various VLSI design concepts - regularity, modularity, and locality.
 - (b) Explain LOCOS technique used for device isolation and state its advantages over the 04 Etched Field Oxidation technique.
 - Explain the behaviour of MOS device under external bias with the help of energy band 07 (c) diagrams and derive the relationship for maximum depletion width at oxidesemiconductor surface.
- (a) Compare ion implantation and diffusion methods used for impurity doping. 03 Q.2
 - (b) Explain the substrate bias effect in nMOS and pMOS devices.
 - Explain the experimental methods of measuring following parameters of nMOS: 07 (c) Threshold voltage (V_T), channel length modulation coefficient (λ), substrate-bias coefficient (γ), transconductance parameter (k_n)

OR

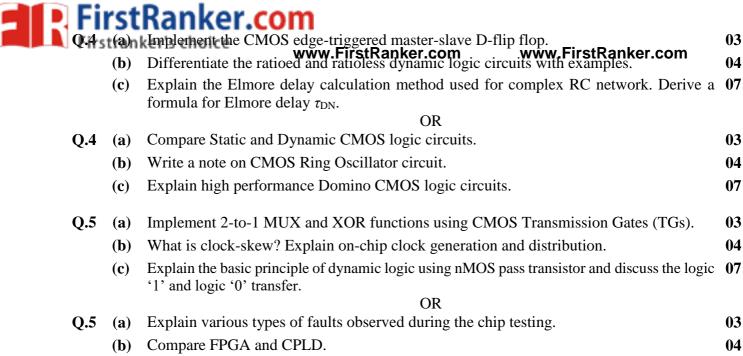
- Consider a MOS system with the following parameters: (c)
 - $t_{ox} = 20 nm$ •
 - $\phi_{GC} = -0.85 V$
 - $N_A = 2 \times 10^5 \ cm^{-3}$
 - $Q_{ox} = q \ge 2 \ge 10^{11} C/cm^2$
 - (i) Determine the threshold voltage, V_{T0} under zero bias at room temperature (T =300 °K). Consider $\varepsilon_{ox} = 3.97 \varepsilon_0$ and $\varepsilon_{Si} = 11.7 \varepsilon_0$
 - (ii)Determine the type (*p*-type or *n*-type) and amount of channel implant (N_I /cm²) required to change the threshold voltage to 0.8 V.
- Explain the effect of noise on the performance of a digital system and define noise 03 Q.3 (a) margins (NM_L and NM_H).
 - Explain resistive load inverter in brief and derive V_{IL} and V_{IH} critical voltage equations **(b)** 04 for this inverter.
 - Explain the MOSFET capacitances in detail. (c)

OR

- Q.3 Draw the nMOS depletion load and CMOS implementations of the following Boolean 03 (a) function : $Y = \overline{A(D+E) + BC}$
 - (b) Explain the latch-up problem observed in CMOS circuits and mention various techniques 04 to prevent it.
 - Consider a CMOS inverter with the following parameters: (c)
 - $V_{DD} = 3.3 V$
 - $V_{T0.n} = 0.6 V$
 - $V_{T0,p} = -0.7 V$
 - $k_n = 200 \, \mu A / V^2$
 - $k_p = 80 \, \mu A / V^2$

Calculate the noise margins of the circuit. Consider $k_R = 2.5 V$ and $V_{T0,n} \neq |V_{T0,n}|$ as it is not a symmetric CMOS inverter.

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Explain the Built-in-Self-Test (BIST) technique for circuit testing. (c)

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