GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VI(NEW) – EXAMINATION – SUMMER 2019

Subject Code:2161101 **Date:18/05/2019**

Subject Name:VLSI Technology & Design

Time:10:30 AM TO 01:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks**

Q.1	**(a)**	Explain various VLSI design concepts - regularity, modularity, and locality.	**03**
	(b)	Explain LOCOS technique used for device isolation and state its advantages over the Etched Field Oxidation technique.	**04**
	(c)	Explain the behaviour of MOS device under external bias with the help of energy band diagrams and derive the relationship for maximum depletion width at oxide-semiconductor surface.	**07**
Q.2	**(a)**	Compare ion implantation and diffusion methods used for impurity doping.	**03**
	(b)	Explain the substrate bias effect in *n*MOS and *p*MOS devices.	**04**
	(c)	Explain the experimental methods of measuring following parameters of *n*MOS: Threshold voltage (V_T), channel length modulation coefficient (λ), substrate-bias coefficient (γ), transconductance parameter (k_n)	**07**
		OR	
	(c)	Consider a MOS system with the following parameters: • $t_{ox} = 20\ nm$ • $\emptyset_{GC} = -0.85\ V$ • $N_A = 2 \times 10^5\ cm^{-3}$ • $Q_{ox} = q \times 2 \times 10^{11}\ C/cm^2$ (i) Determine the threshold voltage, V_{T0} under zero bias at room temperature (T = 300 °K). Consider $\varepsilon_{ox} = 3.97\varepsilon_0$ and $\varepsilon_{Si} = 11.7\varepsilon_0$ (ii) Determine the type (*p*-type or *n*-type) and amount of channel implant (N_I /cm^2) required to change the threshold voltage to 0.8 V.	**07**
Q.3	**(a)**	Explain the effect of noise on the performance of a digital system and define noise margins (NM_L and NM_H).	**03**
	(b)	Explain resistive load inverter in brief and derive V_{IL} and V_{IH} critical voltage equations for this inverter.	**04**
	(c)	Explain the MOSFET capacitances in detail.	**07**
		OR	
Q.3	**(a)**	Draw the *n*MOS depletion load and CMOS implementations of the following Boolean function : $Y = \overline{A(D+E)+BC}$	**03**
	(b)	Explain the latch-up problem observed in CMOS circuits and mention various techniques to prevent it.	**04**
	(c)	Consider a CMOS inverter with the following parameters: • $V_{DD} = 3.3\ V$ • $V_{T0,n} = 0.6\ V$ • $V_{T0,p} = -0.7\ V$ • $k_n = 200\ \mu A/V^2$ • $k_p = 80\ \mu A/V^2$ Calculate the noise margins of the circuit. Consider $k_R = 2.5\ V$ and $V_{T0,n} \neq \lvert V_{T0,p} \rvert$ as it is not a symmetric CMOS inverter.	**07**

Q.4	**(a)**	Implement the CMOS edge-triggered master-slave D-flip flop.	**03**
	(b)	Differentiate the ratioed and ratioless dynamic logic circuits with examples.	**04**
	(c)	Explain the Elmore delay calculation method used for complex RC network. Derive a formula for Elmore delay τ_{DN}.	**07**

OR

Q.4	**(a)**	Compare Static and Dynamic CMOS logic circuits.	**03**
	(b)	Write a note on CMOS Ring Oscillator circuit.	**04**
	(c)	Explain high performance Domino CMOS logic circuits.	**07**
Q.5	**(a)**	Implement 2-to-1 MUX and XOR functions using CMOS Transmission Gates (TGs).	**03**
	(b)	What is clock-skew? Explain on-chip clock generation and distribution.	**04**
	(c)	Explain the basic principle of dynamic logic using nMOS pass transistor and discuss the logic '1' and logic '0' transfer.	**07**

OR

Q.5	**(a)**	Explain various types of faults observed during the chip testing.	**03**
	(b)	Compare FPGA and CPLD.	**04**
	(c)	Explain the Built-in-Self-Test (BIST) technique for circuit testing.	**07**

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