Seat No.: _____ Enrolment No.

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VI(OLD) – EXAMINATION – SUMMER 2019

Subject Code:161004 **Date:20/05/2019**

Subject Name: VLSI Technology And Design

Time:10:30 AM TO 01:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Draw & explain Y Chart.	**07**
	(b)	Explain basic steps of LOCOS isolation with necessary diagram.	**07**
Q.2	**(a)**	Derive the current equation for an n channel MOSFET transistor operating in the saturation region.	**07**
	(b)	Calculate the threshold voltage V_{TO}, for a polysilicon gate n-channel MOS transistor, with the following parameters: Substrate doping density $N_A = 10^{16}$ cm^{-3}, polysilicon gate doping density $N_D = 2x10^{20}$ cm^{-3}, gate oxide thickness t_{ox} = 500Å, and oxide interface fixed charge density $N_{ox} = 4x10^{10}$ cm^{-2}. ($KT/q=0.026V$, $n_i = 1.45x10^{10}$ cm^{-3}, $\varepsilon_0 = 8.85x10^{-14}$ F/cm, $\varepsilon_{Si} = 11.7x\ \varepsilon_0$ F/cm , $\varepsilon_{0x} = 3.97x\ \varepsilon_0$ F/cm)	**07**
		OR	
	(b)	Discuss different operating regions of the MOSFET and derive the equation for the depth of depletion region width.	**07**
Q.3	**(a)**	Draw the inverter circuit with resistive type load. Derive critical voltages points V_{OH},V_{OL},V_{IH} and V_{IL}.	**07**
	(b)	Consider a CMOS inverter circuits with the following parameters: V_{DD}= 3.3V, $V_{T0,n}$ = 0.6V, $V_{T0,p}$ = -0.7V, $k_n = 200uA/v^2$, $k_p = 80uA/v^2$. Calculate the noise margin of the circuit.	**07**
		OR	
Q.3	**(a)**	Explain Elmore delay calculation method for complex RC network. Derive the formula for Elmore delay T_{DN}.	**07**
	(b)	Consider a resistive load inverter circuit with V_{DD} = 5v, $k_n' = 20uA/v^2$, V_{T0} = 0.8v, R_L = 200kΩ and W/L = 2. Calculate the critical voltages V_{OH}, V_{OL}, V_{IH} and V_{IL} on the VTC and find the noise margins of the circuits.	**07**
Q.4	**(a)**	Realize the Boolean function F= [(A(D+E)+BC]' using NMOS depletion load.	**07**
	(b)	Explain in detail CMOS SR latch circuit based on NOR2.	**07**
		OR	
Q.4	**(a)**	Implement F= A XOR B using eight transistor CMOS transmission gate.	**07**
	(b)	Draw CMOS negative edge triggered master slave D flip-flop & explain its working.	**07**
Q.5	**(a)**	Explain the basic principal of pass transistor circuit. Explain Logic '1' transfer and logic '0' transfer.	**07**
	(b)	What is latch up? Mention the causes of the latch-up and its prevention techniques for CMOS inverter.	**07**
		OR	
Q.5	**(a)**	What is the need for voltage bootstrapping? Explain dynamic voltage bootstrapping circuit with necessary mathematical analysis.	**07**
	(b)	Explain in detail: Adhoc testable design techniques.	**07**

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