Seat No.: _____ Enrolment No.

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III (NEW) EXAMINATION – SUMMER 2019

Subject Code: 2131004 **Date: 11/06/2019**

Subject Name:Digital Electronics

Time: 02:30 PM TO 05:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Represent following numbers in 8 Bit Binary representation: **03**
(i) $(126)_{10}$ (ii) $(79)_{10}$ (iii)$(-128)_{10}$

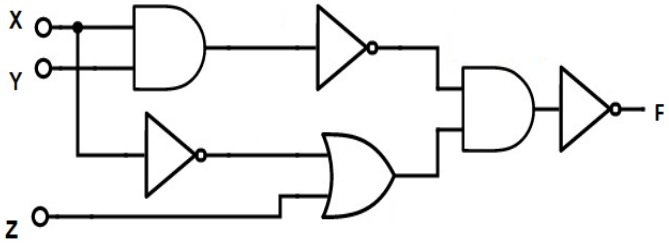
(b) State and explain De Morgan's theorems with truth tables. **04**

(c) Do as directed. **07**

i. Find 8 bit representation of $(-1)_{10}$=(_____)$_2$
ii. Find A+A'B =_____.
iii. _____ and _____ can work as universal gates.
iv. Define term: Propagation Delay
v. By keeping one input HIGH, NAND gate can work as Inverter to second input. (T/F)
vi. Convert $(FFFF)_{16}$=(_____)$_{10}$.
vii. Convert $(125.625)_{10}$=(_____)$_2$.

Q.2 **(a)** Simply Boolean Function : F=A'B'C+A'BC+AB'. **03**

(b) Find the Boolean Equation for following circuit and simplified Boolean equation. **04**



(c) Draw logic circuit of Full Adder and Full Subtractor with truth table. **07**

OR

(c) Generate AND, OR, NOT, EXOR and EX-NOR gate using NAND as a universal gate. **07**

Q.3 **(a)** Obtain canonical Sum of Product form of following function: F=AB+ACD. **03**

(b) Draw logic circuit of 2x4 Decoder. **04**

(c) Simply Boolean function for F(W,X,Y,Z) = Σ (0, 1, 2, 4 ,5 ,6 ,8, 9, 12, 13, 14) **07**

OR

Q.3 **(a)** Explain working of Half Adder circuit with diagram. **03**

(b) Draw logic circuit for 2-Bit Magnitude Comparator. **04**

(c) Design 1-Bit Full Adder using 3x8 Decoder. **07**

Q.4	**(a)**	How to generate 8x1 MUX using 4x1 MUX.	**03**
	(b)	Draw the circuit diagrams and Truth table of all the Flip flops (SR, D).	**04**
	(c)	Derive and draw logic circuit for BCD to Excess-3 Code converter.	**07**

OR

Q.4	**(a)**	Draw logic diagram, graphical symbol and Characteristic table for clocked T flip-flop.	**03**
	(b)	Explain 4-Bit serial in serial out shift register.	**04**
	(c)	Explain working of master-slave JK flip-flop with necessary logic diagram, state equation and state diagram.	**07**
Q.5	**(a)**	Give comparison of TTL and CMOS family.	**03**
	(b)	Draw and explain Ring counter.	**04**
	(c)	Design synchronous counter for sequence: 0→1→3→4→5→7→0 using T flip-flop.	**07**

OR

Q.5	**(a)**	What is race around condition in JK flip flop?	**03**
	(b)	Write short note on Programmable Logic Arrays.	**04**
	(c)	Explain the Fundamental Mode Model of Asynchronous State Machine with suitable example.	**07**

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