Seat No.: _____ Enrolment No.

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VIII(NEW) EXAMINATION – SUMMER 2019

Subject Code:2181107 **Date:09/05/2019**

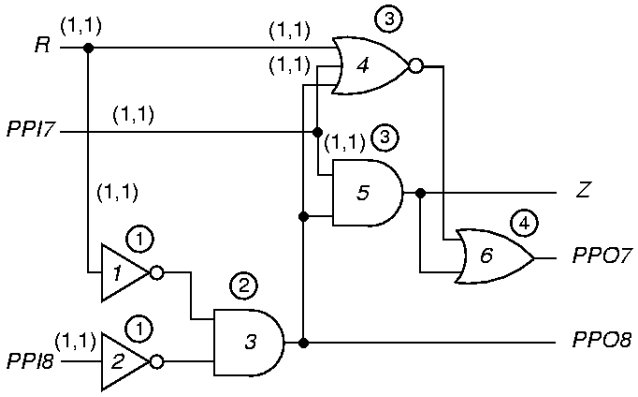
Subject Name:Testing And Verification

Time:10:30 AM TO 01:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

			MARKS
Q.1	**(a)**	Discuss verification versus testing.	**03**
	(b)	List and explain different level of abstraction in VLSI testing.	**04**
	(c)	What is combinational controllability and observability? Find controllability and observability for the following circuit.	**07**



Q.2	**(a)**	Briefly explain different parts and features of ATE.	**03**
	(b)	Write advantages and disadvantages of LSSD scan cell design.	**04**
	(c)	What is Mux-D scan cell design? Explain in detail. Write advantages and disadvantages of Mux-D scan cell design.	**07**
		OR	
	(c)	Define the term: failure mode analyses, failure rate, mean time between failure, mean time to repair, test vector, fault coverage, defect level.	**07**
Q.3	**(a)**	What strategy needs to be applied for verification?	**03**
	(b)	List out different ad-hoc testing technique for VLSI.	**04**
	(c)	Realize stuck at fault with example.	**07**
		OR	
Q.3	**(a)**	What is Functional Verification?	**03**
	(b)	Explain the importance of verification.	**04**
	(c)	The number of failures in 109 hours is a unit (abbreviated FITS) that is often used in reliability calculations. Calculate the MTBF for a system with 500 components where each component has a failure rate of 1000 FITS.	**07**
Q.4	**(a)**	What is compile code simulation?	**03**
	(b)	Compare and contrast different Fault Simulation techniques.	**04**
	(c)	Explain serial fault simulation algorithm with an example.	**07**
		OR	
Q.4	**(a)**	What is event driven simulation?	**03**
	(b)	What is hazard? Explain cause and effect of different types of hazards.	**04**
	(c)	Discuss different delay models.	**07**

Q.5	**(a)**	List different types of test-bench and explain any one.	**03**
	(b)	Discuss different technique for evaluation of logic elements.	**04**
	(c)	Draw and explain test bench architecture.	**07**

OR

Q.5	**(a)**	What is test bench?	**03**
	(b)	Write a test bench for 4 bit shift register.	**04**
	(c)	Write a test bench for 4x1 de-mux.	**07**

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