Seat No.: _____ Enrolment No.

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–IV (NEW) EXAMINATION – WINTER 2018

Subject Code:2141002 **Date:22/11/2018**

Subject Name:Analog Circuit Design

Time: 02:30 PM TO 05:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	State the functions of the transistors connected to the reset and discharge pins of IC 555.	**03**
	(b)	What is the role of the inter electrode capacitances Cbc, Cbe and Cce in a hybrid Π model? Why Cce does not figure in the model?	**04**
	(c)	Define the following for an Op Amp: [1] Input Resistance [2] Slew Rate [3] Balanced output [4] PSRR [5] Voltage Gain [6] Offset Voltage [7] Unity Gain Bandwidth	**07**
Q.2	**(a)**	A bipolar junction transistor has h_{ie}=1 KΩ, h_{fe}= 100; h_{re} , h_{oe} are negligible. Cc=3pF and the collector current is 10mA. The short circuit current gain is 10 at a frequency of 10 M Hz. Calculate the values of f_α, f_β and f_γ.	**03**
	(b)	List all the resistances and their typical values in a hybrid Π model	**04**
	(c)	Draw the hybrid Π model for a single stage CE transistor amplifier having load resistance R_L and obtain the expression for short circuit current gain.	**07**
		OR	
	(c)	Draw the hybrid Π model for a transistor in CE configuration and derive the expression for transconductance g_m. Justify the validity of this model.	**07**
Q.3	**(a)**	Perform DC analysis of a Dual Input Balanced Output Differential Amplifier	**03**
	(b)	For a given operational amplifier, the input voltages are 150 μV and 140 μV DC. This amplifier has a differential gain of 4000 and a CMRR of 100. Evaluate its output voltage. What change would occur in its output voltage if the CMRR changes to a new value of 1,00,000 ?	**04**
	(c)	Define CMRR. Discuss the effect of R_E on CMRR. How can a constant current source and a current mirror circuit help to improve this value?	**07**
		OR	
Q.3	**(a)**	For a dual input balanced output, it is given that V_{CC}= ±12V, R_C=4.7 KΩ, R_B= 100Ω and R_E= 2.7 KΩ. Evaluate its Quiescent point of operation.	**03**
	(b)	What is the significance of Slew Rate? How does it affect the performance of an Op Amp?	**04**
	(c)	Explain the working of an adder and a Subtractor circuit to perform the mathematical operation $V_O=V_1+V_2$ and $V_O=V_1-V_2$ respectively.	**07**
Q.4	**(a)**	What are precision rectifiers? Explain the working of anyone of them.	**03**
	(b)	How does the working of an operational amplifier differ in inverting and noninverting configurations?	**04**
	(c)	Discuss op amp based triangular waveform generator circuits. Obtain the expression for the same.	**07**
		OR	

Q.4	**(a)**	For IC 555, explain the functions of the following pins: [1] Trigger [2] Threshold [3] Control	**03**
	(b)	What is thermal drift and error voltage? Suggest methods to reduce the same.	**04**
	(c)	Explain the compensation of input offset voltage with a neat diagram.	**07**
Q.5	**(a)**	Draw the block diagram of PLL and explain each block.	**03**
	(b)	Discuss the features of LM317 Regulator.	**04**
	(c)	Derive expression of frequency of oscillation of an RC phase shift oscillator.	**07**

OR

Q.5	**(a)**	Derive the expression for filter transfer function of a first order low pass filter and draw its frequency response characteristics.	**03**
	(b)	Discuss any one application of a PLL in modulation signal detection.	**04**
	(c)	Derive expression of frequency of oscillation of a Wein Bridge oscillator.	**07**

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