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GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III (New) EXAMINATION – WINTER 2018

Subject Code:2131704 **Date:05/12/2018**

Subject Name: Digital Logic Circuits

Time: 10:30 AM TO 01:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Design 3 to 8 line decoder with neat sketch and truth table.	**03**
	(b)	Explain ROM with block diagram. Give classification of ROM.	**04**
	(c)	Explain D type edge triggered flip flop in detail.	**07**
Q.2	**(a)**	Design full subtractor with necessary derivation of functions.	**03**
	(b)	What do you mean by universal gates? Implement NOT, AND, OR with both universal gates.	**04**
	(c)	Design 3 bit binary counter using T flip flops.	**07**
		OR	
	(c)	What is the limitation of Clocked RS flip flop? How it can be resolved using J K flip flop.	**07**
Q.3	**(a)**	Explain gray code in detail.	**03**
	(b)	Express the boolean function F = xy + x'z in a product of maxterm form.	**04**
	(c)	Design 4 bit bidirectional shift register with parallel load facility.	**07**
		OR	
Q.3	**(a)**	Give the comparison of 1's and 2's complements.	**03**
	(b)	Show that AB'C+B+BD'+ABD'+A'C = B+C	**04**
	(c)	Design BCD ripple counter.	**07**
Q.4	**(a)**	Convert $(163.875)_{10}$ to binary.	**03**
	(b)	Explain duality principle with suitable example.	**04**
	(c)	Explain arithmetic, logic and shift microoperations.	**07**
		OR	
Q.4	**(a)**	Subtract $(111.111)_2$ from $(1010.01)_2$	**03**
	(b)	Explain DeMorgan theorem with suitable example.	**04**
	(c)	Explain emitter coupled logic with neat sketch.	**07**
Q.5	**(a)**	Simplify the Boolean expression F(A,B,C,D) = Σ(2,3,6,7,8,10,11,13,14) using K Map.	**03**
	(b)	Simplify the Boolean function F(w,x,y,z) = Σ(1,3,7,11,15) with don't care condition d(w,x,y,z) = Σ(0,2,5)	**04**
	(c)	Explain dual slope analog to digital converter.	**07**
		OR	
Q.5	**(a)**	Simplify Boolean function F = A'B'C'+B'CD'+A'BCD'+AB'C' using K map.	**03**
	(b)	Reduce the following expressions F_1 (A,B,C,D)= Σ(1,2,3,6,8,12,14,15) and F_2 (A,B,C,D)= II(0,4,9,10,11,14,15) using K map.	**04**
	(c)	Explain R-2R ladder type digital to analog converter.	**07**

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