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GUJARAT TECHNOLOGICAL UNIVERSITY

oject	GUJAKAT TECHNOLOGICAL UNIVERSITY BE - SEMESTER-III (New) EXAMINATION – WINTER 2018 Code:2131704 Date:05/12/2018	
Subject Name: Digital Logic CircuitsTime: 10:30 AM TO 01:00 PMTotal Marks: 70Instructions:		
1.	Attempt all questions.	
(a) (b) (c)	Design 3 to 8 line decoder with neat sketch and truth table. Explain ROM with block diagram. Give classification of ROM. Explain D type edge triggered flip flop in detail.	03 04 07
(a) (b)	Design full subtractor with necessary derivation of functions. What do you mean by universal gates? Implement NOT, AND, OR with both universal gates.	03 04
(c)	Design 3 bit binary counter using T flip flops.	07
(c)	What is the limitation of Clocked RS flip flop? How it can be resolved using J K flip flop.	07
(a)	Explain gray code in detail.	03
(D) (C)	Design 4 bit bidirectional shift register with parallel load facility. OR	04 07
(a)	Give the comparison of 1's and 2's complements.	03
		04 07
(e) (a)	Convert (163.875) ₁₀ to binary.	03
(b)	Explain duality principle with suitable example.	04
(c)		07
(a)		03
(b)	Explain DeMorgan theorem with suitable example.	04
(c)	Explain emitter coupled logic with neat sketch.	07
(a)	Simplify the Boolean expression $F(A,B,C,D) = \Sigma(2,3,6,7,8,10,11,13,14)$ using K Map.	03
(b)	Simplify the Boolean function $F(w,x,y,z) = \Sigma(1,3,7,11,15)$ with don't care	04
(c)	Explain dual slope analog to digital converter. OR	07
(a)	Simplify Boolean function $F = A'B'C'+B'CD'+A'BCD'+AB'C'$ using K map.	03
(b)	Reduce the following expressions F_1 (A,B,C,D)= $\Sigma(1,2,3,6,8,12,14,15)$ and F_2 (A,B,C,D)= $II(0,4,9,10,11,14,15)$ using K map	04
(c)	$(A,B,C,D) = \Pi(0,4,9,10,11,14,13)$ using K map. Explain R-2R ladder type digital to analog converter.	07
	b ject ne: 1 ructio 1. 2. 3. (a) (b) (c) (a) (b) (c) (a) (b) (c) (a) (b) (c) (a) (b) (c) (a) (b) (c) (a) (b) (c) (a) (b) (c) (a) (b) (c) (a) (b) (c) (a) (b) (c) (a) (b) (c) (c) (a) (b) (c) (c) (a) (b) (c) (c) (c) (a) (b) (c) (c) (c) (c) (c) (c) (c) (c) (c) (c	BE - SEMESTER-III (New) EXAMINATION - WINTER 2018 opter Code:2131704 Date:05/12/2018 opter Name: Digital Logic Circuits ne: 10:30 AM TO 01:00 PM Total Marks: 76 ructions: 1. Attempt all questions. 2. Make suitable assumptions wherever necessary. 3. Figures to the right indicate full marks. (a) Design 3 to 8 line decoder with neat sketch and truth table. (b) Explain ROM with block diagram. Give classification of ROM. (c) Explain ROM with block diagram. Give classification of ROM. (c) Explain D type edge triggered flip flop in detail. (a) Design full subtractor with necessary derivation of functions. (b) What do you mean by universal gates? Implement NOT, AND, OR with both universal gates. (c) Design 3 bit binary counter using T flip flops. 0R (c) What is the limitation of Clocked RS flip flop? How it can be resolved using J K flip flop. (a) Explain gray code in detail. (b) Express the boolcan function F = xy + x'z in a product of maxtern form. (c) Design 4 bit bidirectional shift register with parallel load facility. 0R (a) Give the comparison of 1's and 2's complements. (b) Show that AB'C+B+BD'+ABD'+A'C = B+C (c) Design BCD ripple counter. (a) Convert (163.875) to to binary. (b) Explain duality principle with suitable example. (c) Explain anithmetic, logic and shift functooperations. (c) Explain anithmetic, logic and shift microoperations. (c) Explain emitter coupled logic with neat sketch. (a) Simplify the Boolean expression F(A,B,C,D) = $\Sigma(2,3,6,7,8,10,11,13,14)$ using K Map. (b) Simplify the Boolean function F (w,x,y,z) = $\Sigma(1,3,7,11,15)$ with don't care condition d(w,x,y,z) = $\Sigma(0,2,5)$ (c) Explain dual slope analog to digital converter. (c) R (a) Simplify Boolean function F = A'B'C'+B'CD'+A'BCD'+AB'C' using K map. (b) Simplify Boolean function F = A'B'C'+B'CD'+A'BCD'+AB'C' using K map. (b) Reduce the following expressions $F_1(A,B,C,D) = \Sigma(1,2,3,6,8,12,14,15)$ and F_2 (A,B,C,D) = II(0,4,9,10,11,14,15) using K map.
