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GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER-III (New) EXAMINATION - WINTER 2018 Subject Code:2132003 Date:01/12/2018 Subject Name:Design Concepts in Basic Electronics Time:10:30 AM TO 01:00 PM Total Marks: 70

Instructions:

- 1. Attempt all questions.
- 2. Make suitable assumptions wherever necessary.
- 3. Figures to the right indicate full marks.

0.1	(a)	Evaluin in detail different types of baseledown in diede	02
Q.1	(a)	Explain in detail different types of breakdown in diode.	03
	(b)	What are the factors affecting the stability of Q point?	04
	(c)	Explain DC load line and Q-point for any transistor configuration. Also state	07
		the necessity of biasing and list biasing methods for transistor	
Q.2	(a)	What is energy band diagram?	03
•	(b)	Explain with circuit diagram positive clamper and negative clamper.	04
	(c)	Explain the input output characteristics of n-p-n transistor in CE configuration. Also indicate different regions.	07
		OR	
	(c)	A circuit receive a 4-bit excess-3 code. Design a minimal circuit to detect a	07
		decimal number 0,1,4,6,7 and 8	
Q.3	(a)	Draw and explain internal construction of encoder.	03
	(b)	Explain in detail bidirectional shift register with parallel load	04
	(c)	Design a combinational logic to convert given BCD to seven segment display	07
		LED.	
		OR	
Q.3	(a)	Write the points of difference between combinational and sequential logic.	03
	(b)	Draw the circuit diagram of D-type positive edge triggered flip flop	04
	(c)	Write a note on collector to base bias.	07
Q.4	(a)	What is ripple counter?	03
	(b)	Implement 32x1 Multiplexer using four 8x1 Multiplexer and one 4x1	04
	<u>(</u> -)	Multiplexer	
	(c)	A p-n-p germanium transistor is used in the self biasing arrangement with	07

(c) A p-n-p germanium transistor is used in the self biasing arrangement with 07 VCC = 5V, R1 = 27k, R2 = 3k, RE = 270 Ω , RC = 2k and β = 50. Find VCEQ and ICQ.



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03

04

OR

- **Q.4** (a) Explain with example working of transistor as switch.
 - (b) Design 3- bit up synchronous counter.
 - (c) The fixed bias circuit of Fig. uses a silicon transistor. The component values are $RC = 500 \ \Omega$ and $RB = 100 \ k\Omega$. βdc of the transistor is 100 at 30°C and increases to 120 at a temperature of 80°C. Determine the percent change in the Q point values over this temperature range. Assume that VBE and ICBO remain constant.



Q.5	(a)	Explain the requirement of compliment in digital logic.	03
	(b)	Implement the following function with help of 8x1 Multiplexer. F (A,B,C,D) = $\sum (0,1,3,4,8,9,15)$	04
	(c)	Explain with neat diagram Voltage divider bias	07
Q.5	(a)	Why we require master slave or edge triggered flip flop	03
C	(b)	Write a short note on surface mount transistors.	04
	(c)	Compare in detail RTL, DTL, TTL, ECL and CMOS.	07
