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GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–V (NEW) EXAMINATION – WINTER 2018

Subject Code: 2151007 **Date:04/12/2018**

Subject Name: Digital Design

Time: 10:30 AM TO 01:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

			MARKS
Q.1	**(a)**	Differentiate between concurrent and sequential signal assignment statement.	**03**
	(b)	Explain digital system based on FPGA with necessary diagram.	**04**
	(c)	Describe the major capabilities of VHDL?	**07**
Q.2	**(a)**	What is entity? Explain with example.	**03**
	(b)	Distinguish between signals and variables. Give examples.	**04**
	(c)	Write brief note on VHDL data types.	**07**
		OR	
	(c)	Write a VHDL code for full adder using two half adder and use structure modeling.	**07**
Q.3	**(a)**	What is Delta-delay? What is its effect in VHDL?	**03**
	(b)	Write VHDL code for -ve edge triggered D flip-flop.	**04**
	(c)	Write a VHDL code for barrel shifter.	**07**
		OR	
Q.3	**(a)**	Explain packages and library with example.	**03**
	(b)	Write a VHDL code for 4bit adder using structure modeling.	**04**
	(c)	Explain CPLD Architecture in brief.	**07**
Q.4	**(a)**	Explain transport delay model and inertial delay model.	**03**
	(b)	Write VHDL Code for 1 X 4 DMUX using case statement.	**04**
	(c)	Draw mealy FSM to detect 111 sequence and also write VHDL code.	**07**
		OR	
Q.4	**(a)**	Explain generic and configuration with example.	**03**
	(b)	Write VHDL code for 3x8 decoder using behavioral modeling.	**04**
	(c)	Draw Moore FSM to detect 101 sequence and also write VHDL code.	**07**
Q.5	**(a)**	Explain process statement briefly and write VHDL code for JK FLIPFLOP using behavioral.	**03**
	(b)	Explain test bench with example.	**04**
	(c)	Write a VHDL code for 3 bit shift right register using generate statement.	**07**
		OR	
Q.5	**(a)**	Explain assertion statement with example.	**03**
	(b)	Write a VHDL code for 3 bit counter using generate statement.	**04**
	(c)	Write a VHDL code for 4 Bit Parallel –In-Serial-out Shift Register	**07**

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