Seat No.: _____ Enrolment No.

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VI (NEW) EXAMINATION – WINTER 2018

Subject Code:2161101 **Date:30/11/2018**

Subject Name:VLSI Technology & Design

Time: 02:30 PM TO 05:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain VLSI Design flow using Y-chart.	**03**
	(b)	Discuss physical parameters affecting the threshold voltage of MOS structure.	**04**
	(c)	Derive the MOSFET drain current equation while MOSFET is operating in linear region using GCA.	**07**
Q.2	**(a)**	Draw mask layout of the CMOS Inverter and indicate various terms.	**03**
	(b)	In CMOS inverter circuit, enhancement type MOSFET devices are used and if V_{DD} is reduced below $V_{T0,n} + \|V_{T0,p}\|$, explain how the output voltage will follow the change in input voltage. Draw VTC and explain its behavior.	**04**
	(c)	Discuss fabrication process of n-channel MOSFET in detail.	**07**
		OR	
	(c)	Draw Resistive-load inverter using n-channel MOSFET. Derive expressions of critical voltages V_{OL} V_{OH}, V_{IL}, and V_{IH} of Resistive-load inverter.	**07**
Q.3	**(a)**	Compare Semi-custom and Full custom VLSI design style.	**03**
	(b)	What do you mean by MOSFET Scaling? Explain Constant-field Scaling.	**04**
	(c)	"The average power dissipation of the CMOS Inverter is proportional to switching frequency." Explain it with necessary mathematical analysis.	**07**
		OR	
Q.3	**(a)**	Give comparison between FPGA and CPLD.	**03**
	(b)	Describe Accumulation and Inversion process for the MOS system under external bias.	**04**
	(c)	Derive expression of τ_{PHL} for CMOS Inverter where input is ideal step input.	**07**
Q.4	**(a)**	Explain CMOS Ring Oscillator circuit in brief.	**03**
	(b)	Draw different representations of the CMOS Transmission Gate. Implement 2×1 Multiplexer circuit using two CMOS TGs and one inverter.	**04**
	(c)	Explain cascading problem observed in dynamic CMOS logic. What are the different approaches to solve this problem?	**07**
		OR	
Q.4	**(a)**	Discuss VTC of CMOS Inverter with operating region.	**03**
	(b)	Implement Boolean function Z = AB+C(D+E) using CMOS logic circuit	**04**
	(c)	Discuss need of Voltage Bootstrapping and explain dynamic Voltage Bootstrapping with necessary mathematical analysis.	**07**
Q.5	**(a)**	List out possible physical, electrical and logical faults observed at Chip Testing.	**03**
	(b)	Define *Latch-up*. Enlist guidelines for avoiding Latch-up.	**04**
	(c)	Explain D latch with CMOS implementation.	**07**
		OR	
Q.5	**(a)**	Draw NAND gate based CMOS SR latch circuit.	**03**
	(b)	Explain various Clock Distribution Networks.	**04**
	(c)	Explain Ad Hoc Testable Design Techniques.	**07**

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