Seat No.: _____ Enrolment No.

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VI (OLD) EXAMINATION – WINTER 2018

Subject Code:161004 **Date: 27/11/2018**

Subject Name: VLSI Technology And Design

Time: 02:30 PM TO 05:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

			MARKS
Q.1	**(a)**	Explain VLSI design flow.	**07**
	(b)	Write short note on CMOS Transmission Gates.	**07**
Q.2	**(a)**	Describe fabrication process of MOSFET.	**07**
	(b)	Define following operating regions for the MOS system with suitable energy band diagrams: (a) Accumulation (b) Depletion (c) Inversion	**07**
	(b)	Derive the expression of threshold voltage of an n-channel MOSFET.	**07**
Q.3	**(a)**	Draw CMOS inverter circuit, its VTC and derive V_{IH} and V_{IL}.	**07**
	(b)	Consider a CMOS inverter circuit with the following parameters: V_{DD} = 3.3 V,$V_{To,n}$ = 0.6 V $V_{To,p}$ = - 0.7 V,Kn = 200 µA/V2 , Kp = 80 µA/V2 . Calculate the noise margins of the circuit.	**07**
Q.3	**(a)**	Draw resistive load inverter circuit and derive V_{OH}, V_{OL}, V_{IL}, and V_{IH}.	**07**
	(b)	Design a resistive-load inverter with R = 1 kΩ, such that V_{OL} = 0.2 V. The enhancement-type nMOS driver transistor has the following parameters VDD = 5 .0 V V_{TO}= 1. V µnCox = 30 µA/V^2 Determine the required aspect ratio, W/L.	**07**
Q.4	**(a)**	Define propagation delay and derive the expression for τ_{PHL} for CMOS Inverter. Assume ideal step as an input to CMOS Inverter.	**07**
	(b)	Explain the basic principle of pass transistor circuit. Explain logic ‘1’ transfer and logic ‘0’ transfer.	**07**
Q.4	**(a)**	Write a note on CMOS Ring Oscillator circuit.	**07**
	(b)	Explain the dynamic CMOS logic (Precharge – Evaluation) and discuss the cascading problem in dynamic CMOS logic.	**07**
Q.5	**(a)**	Implement following Boolean logic equation using Transmission Gate (TG). Y = AB+ A’C’+AB’C	**07**
	(b)	Discuss the on-chip clock generation and distribution.	**07**
Q.5	**(a)**	Explain Built In Self Test (BIST) in detail.	**07**
	(b)	Give comparison between FPGA and CPLD.	**07**

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