

GUJARAT TECHNOLOGICAL UNIVERSITY**BE - SEMESTER-III (OLD) EXAMINATION – WINTER 2018****Subject Code:130701****Date:22/11/2018****Subject Name:Digital Logic Design****Time:10:30 AM TO 01:00 PM****Total Marks: 70****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

- Q.1** (a) With neat logical diagram & truth table explain all the basic gates including NAND, NOR, EX-OR, EX-NOR gate. **07**
(b) Convert $(4BAC)_{16} = (\text{_____})_8 = (\text{_____})_4 = (\text{_____})_2 = (\text{_____})_{10}$ **07**
- Q.2** (a) State and prove Demorgan's theorem. **07**
(b) Simplify the following Boolean function using k-map **07**
(i) $F(w, x, y, z) = \sum m(0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$
(ii) $F(x, y, z) = \sum m(0, 1, 3, 4, 5, 7)$
OR
(b) Design a full adder circuit using two half adders & gates. **07**
- Q.3** (a) Simplify following Boolean function by using the tabulation method **07**
 $F(w, x, y, z) = \sum m(0, 1, 2, 8, 10, 11, 14, 15)$
(b) Using the law of Boolean algebra prove that **07**
(i) $AB + BC + A'C = AB + A'C$ (ii) $A [B + C (AB + AC)'] = AB$.
OR
- Q.3** (a) Design and explain a logic diagram of 3 to 8 Decoder. **07**
(b) Design and explain 4 x 1 Multiplexer. **07**
- Q.4** (a) Draw & explain T Flip Flop & D Flip Flop. **07**
(b) Realize the expression $F(A, B, C, D) = \sum m(4, 6, 7, 8, 9, 12, 14, 15)$ using an 8:1 MUX. **07**
OR
- Q.4** (a) Write a note on Binary Ripple Counter. **07**
(b) Explain JK Flip Flop with its characteristic table. **07**
- Q.5** (a) Write a short on Hard – Wire Control. **07**
(b) Design a circuit for Binary to Gray code conversion. **07**
OR
- Q.5** (a) Explain Macro Operation v/s Micro Operation. **07**
(b) Implement Full Subtractor circuit with the help of Decoder & logic gates. **07**
