Seat No.: _____ Enrolment No.

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VIII (NEW) EXAMINATION – WINTER 2018

Subject Code: 2181107 **Date: 15/11/2018**

Subject Name: Testing And Verification

Time: 02:30 PM TO 05:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

			MARKS
Q.1	**(a)**	Define or briefly explain following terms: 1. Reliability 2. Repair time 3. Rule of ten	**03**
	(b)	Discuss the Transport Delay, Inertial Delay, wire delay and functional element delay in brief.	**04**
	(c)	Discuss combinational testability analysis by using necessary equation of controllability and observability.	**07**
Q.2	**(a)**	Explain the importance of verification.	**03**
	(b)	Write the types of test bench and explain any one of them.	**04**
	(c)	Draw and explain Enhanced Scan Architecture.	**07**
		OR	
	(c)	Draw Muxed-D scan cell and explain full-scan design approach with necessary diagram using this scan cell.	**07**
Q.3	**(a)**	What is the importance of Test Point Insertion approach?	**03**
	(b)	Draw LSSD (Level sensitive scan design) scan cell design and explain its operation with help of waveforms.	**04**
	(c)	What do you understand by stuck-at-faults? Draw half-adder circuit and discuss all possible stuck-at-faults for this circuit as well as find a set of optimum test vectors to detect these stuck-at-faults.	**07**
		OR	
Q.3	**(a)**	Determine probability based controllability and observability for 3 inputs OR gate.	**03**
	(b)	Draw clocked scan cell design and explain its operation with help of waveforms.	**04**
	(c)	Discuss all possible transistor faults in two-input CMOS NOR gate and the method of testing each of them.	**07**
Q.4	**(a)**	Write a VHDL/Verilog test bench for 4 X 1 Mux.	**03**
	(b)	Define Hazard. List out different type of Hazard.	**04**
	(c)	Discuss the deductive fault simulation.	**07**
		OR	
Q.4	**(a)**	Write a VHDL/Verilog test bench for half adder.	**03**
	(b)	Define Logic Element Evaluation. Explain any one type of Logic Element Evaluation technique.	**04**
	(c)	Discuss the two pass event driven simulation. Explain in detail.	**07**

Q.5	**(a)**	Explain scan design rule for Gated clock design style.	**03**
	(b)	Explain the levels of verification.	**04**
	(c)	Explain the verification plan.	**07**

OR

Q.5	**(a)**	Explain scan design rule for Derived clock design style and give recommended solution.	**03**
	(b)	Explain the architecture of test bench	**04**
	(c)	Explain the verification flow.	**07**

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