Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VIII(OLD) EXAMINATION – WINTER 2017

Subject Code: 180802 **Date: 02-11-2017**

Subject Name: VLSI Technologies

Time: 02:30 pm TO 5:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q-1	**(a)**	Explain the VLSI design flow by Y-chart and its simplified view	**7**
	(b)	Discuss basic steps of fabrication.	**7**
Q-2	**(a)**	Explain Channel Length Modulation	**7**
	(b)	Explain energy band diagram of MOS structure at surface inversion and derive the equation of threshold voltage.	**7**
		OR	
Q-2	**(b)**	Derive the expression for drain current as a function of VGS, VDS and VSB for all three region of operation of MOSFET using Gradual Channel Approximation.	**7**
Q-3	**(a)**	Explain the functioning of depletion load nMOS inverter and derive critical voltage points VOH, VOL, VIL and VIH.	**7**
	(b)	Give the delay time definitions and calculation of delay times.	**7**
		OR	
Q-3	**(a)**	Draw two types of enhancement – load n-MOS inverter circuits and compare both.	**7**
	(b)	Write a short note on MOSFET Capacitance.	**7**
Q-4	**(a)**	Concept of regularity, modularity and locality.	**7**
	(b)	Explain Device Isolation Technique and Locos.	**7**
		OR	
Q-4	**(a)**	Write a short note on FPGA.	**7**
	(b)	Explain CMOS Transmission gates (or Pass Gates).	**7**
Q-5	**(a)**	Ad HOC testable design techniques	**7**
	(b)	Explain the basic principle of pass transistor circuit. Explain logic "1" transfer and logic "0" transfer.	**7**
		OR	
Q-5	**(a)**	Explain the criteria to measure the design quality to improve the chip design and explain any two in brief.	**7**
	(b)	Write a short note on Built In Self Test (BIST).	**7**
