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GUJARAT TECHNOLOGICAL UNIVERSITY

BE – SEMESTER VIII((OLD)) • EXAMINATION – WINTER 2017

Subject Code:181104 **Date: 02-11-2017**

Subject Name: Advanced Microprocessor

Time: 02:30 pm to 05:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	1. Explain the difference between the IDIV and DIV instruction.	**02**
		2. How many bytes of memory store a far direct jump instruction? What is stored in each of the bytes?	**02**
		3. How Physical address is generated in 8086?	**01**
		4. Why local variables are required in macro? How to define local variables in macro?	**02**
	(b)	Explain following 8086 instruction description (i) SCASB (ii) TEST (iii) LOOPE (iv) LOCK and directives description of (i) EQU (ii) EVEN (iii) EXTRN.	**07**
Q.2	**(a)**	Draw the interfacing diagram for 8086 base system configured in maximum mode with following specifications. (i) 8086 working at 5MHz (ii) 16 KB EPROM device (iii) 32 KB SRAM device to include IVT. Use full decoding technique. Draw memory map for above interface.	**07**
	(b)	Describe in brief about following of 8086 microprocessor. (i) EU (ii) BIU	**07**
		OR	
	(b)	1.Explain the function of following pins in 8086 (i) NMI (ii) $\overline{BHE}$ (iii) DEN (iv) QS_0-QS_1	**04**
		2. Describe the significance of queue in 8086	**03**
Q.3	**(a)**	Explain 8086 microprocessor in maximum mode configuration with diagram.	**07**
	(b)	Draw interrupt vector table. Briefly describe the conditions which cause the 8086 to perform each of the following types of interrupts: Type 0, Type 1, Type 2, Type 3 and Type 4.	**07**
		OR	
Q.3	**(a)**	Write an assembly language program in 8086 to find the Factorial of a Number using Recursive procedure.	**07**
	(b)	Write an assembly language program in 8086 to sort the numbers in ascending order	**07**

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Q.4	**(a)**	What do you mean understand by Address Decoding? List various techniques of Address Decoding for Memory interfacing using 8086 and explain any two among them.	**07**
	(b)	Explain VERW, ARPL, VERR, LSL instruction of 80286.Why does the 80286 need to have more instructions than the 80186?	**07**

OR

Q.4	**(a)**	What are the various ways of segment privilege level protection in 80386 microprocessor? Explain the operation of call gate mechanism in detail to change privilege levels	**07**
	(b)	What is virtual mode addressing? What are the steps taken in moving to protected mode from real mode?	**07**
Q.5	**(a)**	List the types of Descriptors. Explain the task state segment descriptor in detail. How does it differ from gate descriptor?	**07**
	(b)	Explain paging mechanism. Explain the page table and page directory entry with example of 80386 processor	**07**

OR

Q.5	**(a)**	Explain EFLAG register of 80486 in detail. What differences exist in the flags of the 80486 when compared to the 80386 microprocessor?	**07**
	(b)	Describe the five stage pipeline mechanism and branch prediction logic in detail for Pentium System.	**07**

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