SY-IT

DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE

Mid Semester Examination – Sept./Oct. 2019

Course: B. Tech in Information Technology **Sem: III**

Subject Name: Computer Architecture & Organization **Subject Code: BTCOC304**

Max Marks: 20 **Date:- 07/10/2019** **Duration:- 1 Hr.**

Instructions to the Students:

1. Assume suitable data wherever necessary and mention it clearly.
2. Figures to right indicate full marks.

	(Level/CO)	Marks
Q. 1 Attempt the following.		**1 X 6**
1. Write 2's complement representation of -10 and +10. A) 0110, 1010 B)1010, 0110 C) 0101, 1010 D) 1010, 0101	CO1	
2. What is the result of multiplication of unsigned integers 1011 x 1101. A) 0001111 B) 10011111 C)10001111 D) 00001111	CO1	
3. How many representations are there for 0 (zero) in 1's compliment representation. A) One B) Two C) Three D) No Representation	CO1	
4. The interconnection mechanism that connects major computer components (processor, memory, I/O) is called_____ A) Component Bus B) System Bus C) Main Bus D) Major Bus	CO1	
5. Assembler directives are commands that are understood by the_____ A) Compiler B) Assembler C) CPU D) Control Unit	CO1	
6. Instruction register (IR), contains the 8-bit opcode instruction being executed. The statement is: A) True B) False	CO1	

Q.2	**Solve Any Two of the following.**		**3 X 2**
(A)	Draw and explain von-Neuman's architecture.	CO3	
(B)	Explain any two addressing modes with diagram.	CO1	
(C)	Differentiate between RISC and CISC architecture.	CO3	
Q. 3	**Solve Any One of the following.**		**8 X 1**
(A)	Sketch and explain flowchart for Booth's algorithm.	CO4	
(B)	Explain in detail data flow during an instruction cycle.	CO4	

***** End *****