Roll No. ☐☐☐☐☐☐☐☐☐☐☐   Total No. of Pages : 02

Total No. of Questions : 09

B.Tech.(ECE/ (2012 to 2017)/B.Tech.(Electronics & Telecom Engg.)
(Sem.–5)
LINEAR INTEGRATED CIRCUITS
Subject Code : BTEC-503
M.Code : 70547

Time : 3 Hrs.   Max. Marks : 60

INSTRUCTIONS TO CANDIDATES :
1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

1. **Answer briefly :**

   a) Draw sample and hold circuit.

   b) What is a Voltage follower?

   c) Draw the circuit of peak detector.

   d) Define CMMR.

   e) Why switching regulators have better efficiency than series regulators?

   f) Draw the non inverting op-amp circuit diagram.

   g) What is the main advantage of constant current bias over emitter bias in differential amplifiers?

   h) What is the purpose of low pass filter in a phase locked loop?

   i) What are the effects of voltage series feedback in Op-amp?

   j) What is the use of all pass filter?

SECTION-B

2. Draw the op-amp block diagram and explain the functions of each block.

3. Explain the concept of level translator.

4. Draw the functional block diagram of IC 555 in detail.

5. Explain the operation of Narrow band pass filter with a neat diagram.

6. Explain how the average circuit can be derived from the summer.

SECTION-C

7. Derive the Differential Amplifier- AC analysis of single input dual output Configuration in detail.

8. Draw the block diagram of Astable operations using IC 555 and derive its time constant.

9. Design and draw the circuit diagram of a second order low pass Butterworth filter having a high cut-off frequency of 1kHz. Use capacitor value $\leq 1\mu F$.

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.