Roll No. | | | | | | | | | | | | |

Total No. of Pages : 02

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B.Tech.(ECE) (2012 to 2017) (Electronics & Telecom Engg.)
(Sem.–6)

VLSI DESIGN

Subject Code : BTEC-604
M.Code : 71124

Time : 3 Hrs. **Max. Marks : 60**

INSTRUCTION TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

1. Answer briefly :

a. What are the different architectural style of VHDL?

b. What is the difference between transport and inertial delay?

c. Write the syntax for the package body.

d. What do you understand by the term entity?

e. Using data flow design, design 2 input XOR gate.

f. What is scaling of MOS circuit?

g. What is noise margin?

h. Define Overloading

i. Differentiate between PLA and PAL

j. Write the syntax for while loop

SECTION-B

2. Write VHDL code for the full adder in structural modeling.
3. Define NMOS inverter. Draw and explain the transfer characteristics.
4. Illustrate the use of package declaration and package body with an example.
5. Write the VHDL code for D flip flop.
6. Write VHDL code for BCD to 7 segment decoder using CASE statement.

SECTION-C

7. Draw and explain MOS structure. Derive the MOS device design equation.
8. Differentiate between NMOS, PMOS and CMOS.
9. Write the VHDL code for 4:1 MUX using different type of architecture techniques.

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.