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Roll No. | | | | | | | | | | | | | Total No. of Pages : 02

Total No. of Questions : 09

B.Tech (ECE) (2012 to 2017 E-III) (Sem.–7,8)

COMPUTER ORGANIZATION AND ARCHITECTURE

Subject Code : BTEC-914

M.Code : 71814

Time : 3 Hrs. Max. Marks : 60

INSTRUCTIONS TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

1. Answer briefly :

a) How memory interleaving is different from cache memory?

b) What is the purpose of prefetch buffers in instruction pipelining?

c) What are the trade offs in scalability analysis?

d) What is meant by inclusion, coherence and locality in a memory hierarchy?

e) What is a sector mapping cache?

f) How multithreading is different from superscalar architecture?

g) What are the limitations of parallel processing?

h) What do you understand by MFLOPS?

i) What is PCI express?

j) What is semiconductor memory?

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SECTION-B

2. How an instruction is executed? Explain with the help of instruction cycle.

3. What is an interrupt? What are the various types of interrupt? Explain with example

4. How parallelism is achieved in micro instructions? Discuss.

5. Distinguish between single threaded and multithreaded processor architecture.

6. Describe the language features needed for parallel programming.

SECTION-C

7. What is memory Organization? What is the different hierarchy of memory?

8. What is meant by Cache-Only Memory Architecture (COMA) model? How is it different from non-uniform-memory-access model?

9. What are the features of Hardwired control and micro programmed control? Discuss.

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NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.

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