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Total No. of Questions : 09

B.Tech (ECE) (Sem.-7)
VLSI DESIGN & TECHNOLOGY
Subject Code : EC-406
M.Code : 57555

Time : 3 Hrs.

Max. Marks : 60

INSTRUCTIONS TO CANDIDATES :

1. **SECTION-A** is **COMPULSORY** consisting of **TEN** questions carrying **TWO** marks each.
2. **SECTION-B** contains **FIVE** questions carrying **FIVE** marks each and students have to attempt any **FOUR** questions.
3. **SECTION-C** contains **THREE** questions carrying **TEN** marks each and students have to attempt any **TWO** questions.

SECTION-A

1. **Write briefly :**
 - a. Enlist different types of delays in VHDL.
 - b. What is difference between signal assignment and variable assignment?
 - c. Enlist the three forms of primary storage in computer.
 - d. Enlist different types of delays in VHDL.
 - e. What is FPGA? What are the main advantages of using FPGA?
 - f. What is role of HDL in digital system design? How does HDL differ from other software language?
 - g. Write a short note on ROM.
 - h. What is Data object? Enlist all types of Data objects.
 - i. What is difference between Encoder & Multiplexer?
 - j. How do you differentiate between Primary Memory and Secondary Memory?

SECTION-B

2. Differentiate between Behavioural and structural styles of Modeling.
3. In Behavioral Modeling explain :
 - a. Architecture Body
 - b. Process statement
 - c. Case statement.
4. Write a VHDL code for 3 bit binary to Excess-3 code converter in Data Flow Modeling?
5. Write a VHDL code for Modulo-5 counter in Structural Modeling.
6. Write a short note on (i) GAL (ii) CPLD

SECTION-C

7. What are the basic components of a computer? Write down VHDL code for Memory Subsystem.
8. What is difference between PAL and PLA? Implement Full Subtractor using PAL.
9. Write a VHDL code for Priority Encoder in Behavioural Modeling and Data Flow Modeling.

NOTE : Disclosure of identity by writing mobile number or making passing request on any page of Answer sheet will lead to UMC case against the Student.