

www.FirstRanker.com

www.FirstRanker.com

Roll No.	Total No. of Pages: 02
----------	------------------------

Total No. of Questions: 09

MCA (2015 & Onward) (Sem.-6) ADVANCED COMPUTER ARCHITECTURE

Subject Code : MCA-603 M.Code : 74757

Time: 3 Hrs. Max. Marks: 60

INSTRUCTIONS TO CANDIDATES:

- SECTIONS-A, B, C & D contains TWO questions each carrying TEN marks each and students has to attempt any ONE question from each SECTION.
- SECTION-E is COMPULSORY consisting of TEN questions carrying TWENTY marks in all.

SECTION-A

- Explain the instruction set architecture in detail.
- a) Describe the working of pipelined processor.
 - b) What are different hazards of pipeline? Explain.

SECTION-B

- a) What is direct mapped memory? Explain by taking example.
 - Explain the working of pipelined cache.
- Describe the concept of write-back and write-through cache by taking suitable examples.

SECTION-C

- a) What are advanced processors? Describe the concept of superscalar execution.
 - b) Define memory disambiguation. Discuss its use.
- What is meant by dynamic instruction scheduling? Also explain the working of SIMD processor.

SECTION-D

- What is meant by memory protection? Why is it required? Also explain the concept of virtualization.
- a) Define Memory synchronization
 - b) Elaborate consistency and coherence

1 M-74757 (S6)-2065





SECTION-E

9. Write briefly:

- a) Comment on hardwired design.
- b) What are multicore processors?
- c) What is meant by pipeline hazard?
- d) Define FSM.
- e) What is the way of measuring the performance of memory?
- Discuss briefly about cache memory.
- g) What is register naming?
- h) What is meant by branch prediction?
- i) What are non-blocking caches?
- j) Discuss the use of virtual memory.

NOTE: Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.

2 | M-74757 (S6)-2065

