Roll No. ☐☐☐☐☐☐☐☐☐☐☐☐ Total No. of Pages : 02

Total No. of Questions : 18

B.Tech. (ECE) (2012 to 2017 E-III)/(Automation & Robotics) (Sem.–7)

COMPUTER ORGANIZATION AND ARCHITECTURE

Subject Code : BTEC-914

M.Code : 71814

Time : 3 Hrs. Max. Marks : 60

INSTRUCTIONS TO CANDIDATES :

1. SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.
2. SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.
3. SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.

SECTION-A

Answer briefly :

1. What is the concept of grain size?
2. What are Superscalar processors?
3. What are the cache addressing models? Name them.
4. What is pipelining?
5. What is the need of cache memory?
6. What is snoopy cache protocol?
7. What is vector processing?
8. Name the types of machines according to the Flynn's Taxonomy.
9. What is the main advantage of pipelining?
10. What are clusters?

SECTION-B

11. What are the Performance metrics? Explain.

12. Explain Pentium 4 Cache Organization.

13. What are Chip Multi-Processors? Explain.

14. Explain the concept of Microinstruction sequencing.

15. How Performance may enhance via pipelining? Explain.

SECTION-C

16. Explain the Flynn's classification in detail.

17. Discuss implementation of the control unit in detail.

18. Discuss Multi-Processor Organization in detail.

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.