

**Total No. of Pages : 02**

**Total No. of Questions : 18**

**B.Tech. (ECE) (Sem.-7)**

# CMOS BASED DESIGN

**Subject Code : BTEC-908**

**M.Code : 71912**

**Time : 3 Hrs.**

**Max. Marks : 60**

**INSTRUCTIONS TO CANDIDATES :**

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

## SECTION-A

**Write briefly :**

- 1) Design a 3 input NOR gate using CMOS inverter.
- 2) Explain pull-up and pull-down networks for CMOS logic.
- 3) Draw drain current vs. voltage chart for MOS transistor.
- 4) Give the steps of CMOS processing.
- 5) Define photolithography.
- 6) Define propagation delay time.
- 7) What do you mean by linear delay model?
- 8) Define circuit family.
- 9) Explain glitching transitions.
- 10) Define the term sizing.

### SECTION-B

- 11) Give various design layout rules.
- 12) Explain the process of Photo masking with a negative resist.
- 13) Enlist the advantages and disadvantages of scaling.
- 14) Using static CMOS, design Bubble pushing to convert ANDs and ORs to NANDs and NORs.
- 15) Explain the optimization of Domino logic.

### SECTION-C

- 16) Explain all the steps of fabrication process with diagrams.
- 17) Explain Gate and shallow source/drain formation.
- 18) Explain transistor and interconnect scaling.

**NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.**