Roll No. | | | | | | | | | | | | |

Total No. of Pages : 02

Total No. of Questions : 18

B.Tech.(EE) PT (Sem.–3)

DIGITAL ELECTRONICS

Subject Code : BTEE-404

M.Code : 72164

Time : 3 Hrs. Max. Marks : 60

INSTRUCTION TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

Answer briefly :

1) Convert Decimal Number 4587 into Octal and Hexadecimal Number systems.

2) Subtract 21 from 36 using 2's complement method.

3) State and prove Demorgan's Theorem.

4) Convert AB + A′B′ into POS form.

5) Define MOD counters.

6) Draw a VHDL view of a Digital model.

7) What do you mean by Figure of merit in Logic family?

8) Define accuracy of D/A converters.

9) Differentiate between RAM and ROM.

10) Define content addressable memories.

SECTION-B

11) Design a 3 bit odd parity generator.

12) Minimize the following expression using Q-M method

$Y = \sum m (1, 2, 3, 6, 7, 9, 10, 11, 13)$

13) Design SR flip flop using JK flip flop.

14) Write a VHDL code for full adder.

15) Draw and explain dual slop A/D converter.

SECTION-C

16) Differentiate between various types of ROM.

17) Explain FPGA in detail.

18) Design universal shift register.

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.