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Roll No. Total No. of Pages: 02

Total No. of Questions: 18

B.Tech. (CSE/IT) (2018 Batch) (Sem.-3)

DIGITAL ELECTRONICS
Subject Code: BTES-301-18

M.Code: 76435

Time: 3 Hrs. Max. Marks: 60

INSTRUCTIONS TO CANDIDATES:

- SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.
- 2. SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.
- 3. SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.

SECTION-A

Write briefly:

- 1. State flip flop and its function.
- 2. Draw the full adder circuit using half adder.
- 3. Write the function of magnitude comparators
- 4. Draw the NOR gate latch write its truth table.
- 5. What are the types of programmable logic devices?
- 6. Give the difference between Moore and Melay's model.
- 7. State the De Morgan's law and write any one application.
- 8. Convert the decimal number 39.75 to hexadecimal.
- 9. Differentiate between combinational circuit and sequential circuits.
- 10. What will be memory capacity of RAM if it has 10 bit address lines?

1 M-76435 (S2)- **644**



SECTION-B

- 11. Compare various number system in detail.
- 12. Illustrate the design procedure with algorithmic state machine with neat flow chart.
- 13. Discuss the features and functional blocks of FPGA.
- 14. Simplify the Boolean expression using K map:

$$F(A,B,C,D) = \Sigma(0,3,6,7,9,13,14,15)$$

15. How an op-Amp will act as differentiator and integrator? Explain.

SECTION-C

- 16. Design AND-OR logic for the expression (A + B)(C + D)(E + F). Also convert the same circuit in NOR logic gate circuit.
- 17. a) What are the different logic gates? Give their truth tables.
 - b) Describe the classification of semiconductor memories.
- 18. What is JK flip flop? Discuss its working. What is race around condition?

NOTE: Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.

2 | M-76435 (S2)- 644