Roll No. | | | | | | | | | | | | | Total No. of Pages : 02

Total No. of Questions : 18

B.Tech. (ECE) (Sem.–3)

DIGITAL SYSTEM DESIGN

Subject Code : UC-BTEC-302-19

M.Code : 78747

Time : 3 Hrs. Max. Marks : 60

INSTRUCTION TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

Answer briefly :

1) Convert decimal number 23.5 into binary, octal and hexadecimal number system.

2) Realize A'B + AB' using NAND gates only.

3) Enlist various steps to subtract two numbers using 2's complement.

4) Draw 3 bit odd parity generator.

5) Design 8:1 multiplexer using 2:1 multiplexer.

6) Write all the decimal digits using seven segment display.

7) What are excitation tables? Write excitation tables of all the flip flops.

8) Draw all types of shift registers.

9) Draw binary ladder D/A converter.

10) What are the capabilities of VHDL?

SECTION-B

11) Minimize the following expression using Q-M method :

$Y = \sum m(0, 2, 5, 7, 8, 10, 13, 15)$

12) Design Gray to Excess-3 code converter.

13) Convert JK flip flop into T flip flop.

14) Write a VHDL code for 4:1 Multiplexer.

15) Draw and explain Random Access Memory.

SECTION-C

16) Design 3 bit up synchronous counter and draw its state diagrams.

17) Explain counter type A/D converter and its working.

18) Realize a 4 variable function using 8:1 multiplexer.

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.