

[B19 CS 1202]

I B. Tech II Semester (R19) Regular Examinations
DIGITAL LOGIC DESIGN
 (Common to CSE & IT)
MODEL QUESTION PAPER

TIME: 3 Hrs.

Max. Marks: 75 M

Answer **ONE Question** from **EACH UNIT**

All questions carry equal marks

			CO	KL	M
UNIT - I					
1.	a).	i. Convert $(1032.2)_4$ to decimal. ii. Perform the subtraction using 2's complement $100-110000$	C1	K2	8
	b).	Reduce the Boolean Functions to minimum number of literals (i) $ABC+A^1B^1C+A^1BC+ABC^1+A^1B^1C^1$ to five literals (ii) $(A+C+D)(A+C+D^1)(A+C^1+D)(A+B^1)$ to fr literals	C1	K2	7
OR					
2.	a).	Convert the function to another canonical form. $F(x,y,z)=\pi(0,3,6,7)$	C1	K2	8
	b).	Implement the Boolean function $F=xy+x^1y^1+y^1z$ with (i) AND ,OR and NOT gates (ii) OR,NOT gates (iii) AND, NOT gates	C1	K2	7
UNIT - II					
3.	a).	Simplify the Boolean Function using K-Map. $F(A,B,C,D)=ACE+A^1CD^1E+A^1C^1DE$ $D(A,B,C,D)=DE^1+A^1D^1E+AD^1E^1$	C2	K3	8
	b).	Design and explain Binary Adder/ Subtractor.	C2	K3	7
OR					
4.	a).	Simplify the Boolean Function to product of sums. $F(A,B,C,D)=\pi(0,1,2,3,4,10,11)$	C2	K2	8
	b).	Design and explain Decimal Adder.	C2	K2	7
UNIT - III					
5.	a).	Design and explain abt JK Flip flop.	C3	K3	8
	b).	Explain abt State Reduction and Assignment with example.	C3	K3	7
OR					
6.		Explain abt design procedure of sequential circuits with an example	C3	K4	15
UNIT - IV					
7.	a).	Design and explain abt Shift Register.	C4	K3	8
	b).	Design and explain abt BCD Ripple cnter .	C4	K3	7
OR					
8.	a).	Design and explain abt Universal Shift Register.	C4	K3	8
	b).	Design and explain abt Synchrons Binary cnter.	C4	K3	7
UNIT - V					
9.	a).	Explain abt Memory decoding of RAM.	C5	K3	8
	b).	Explain abt ROM Variants	C5	K3	7
OR					
10.	a).	Explain PLA and PAL	C5	K3	8
	b).	Explain abt Hamming code with an example	C5	K3	7