Code: 17F00202

MCA II Semester Regular & Supplementary Examinations May/June 2019

COMPUTER ORGANIZATION

(For students admitted in 2017 & 2018 only)

Time: 3 hours Max. Marks: 60

Answer all the questions

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1 (a) Explain the logic diagram of a 4-bit adder-subtractor and explain with the help of a truth table.
(b) Explain the process of floating point number multiplication with a diagram.

OR

2 (a) Explain the hardware for a 2 bit-by-2bit array multiplier and explain its working.
(b) Draw a flow chart that explains the complete operations of how an instruction is fetched, decoded and executed in a computer.

3 (a) Explain memory address map with example.
(b) Explain read and write operations with respect to associative memories.

OR

4 (a) Explain various addressing modes with example.
(b) What is mapping function? What are the ways the cache can be mapped? Explain.

5 (a) Explain design of multiplier control unit using any hardwired design method.
(b) For a single bus organization of CPU, write micro-operations and control signals for unconditioned branch instruction.

OR

6 (a) Write a program to avaluate the arithmetic statement:
X = (A+B)* (C+D)
(i) Using an accumulator type computer with one address instruction.
(ii) Using two or three address instructions.
(iii) Using stack-organized computer with zero address instructions.
(b) Explain Flag transfer and address transfer.

7 (a) Explain block diagram of an Asynchronous communication interface and explain its operation in detail.
(b) Explain memory interface circuit.

OR

8 (a) Differentiate I/O versus memory bus.
(b) Explain: (i) Interrupt cycle. (ii) DMA control. (iii) Modes of transfer.

9 (a) What is interprocessor synchronization? Explain.
(b) What is parallel processing? Explain its mechanism.

OR

10 (a) Explain RISC pipeline.
(b) Explain interconnection structure for multiprocessor systems.

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