Code: 17F00202

MCA II Semester Regular Examinations June/July 2018

COMPUTER ORGANIZATION

(For students admitted in 2017 only)

Time: 3 hours Max. Marks: 60

Answer all the questions

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1 What is meant by decoder? Explain 3 – to – 8 line decoder with diagram and truth table.

OR

2 Design a combination circuit for a full subtractor and explain it in detail.

3 Explain the read and write operations with respect to the association memory. Discuss RAM and ROM chips with diagrams.

OR

4 List out the factors that determine the storage device performance in main memory and 128 blocks in cache with 16 blocks per cache.

5 (a) Which data structures can be the best supported using:
(i) Indirect addressing mode.
(ii) Auto increment/auto decrement addressing mode.

(b) Explain one-address, 2-address and 3-address instructions related to CPU organizations.

OR

6 Write an ALP using 8086 instructions to generate and add the first 10 even numbers and save the numbers and result in memory location num and sum.

7 (a) Compare I/O versus memory bus.

(b) Briefly explain about the daisy-chaining process of prioritizing interrupts.

OR

8 Explain in detail about interrupt handling.

9 How the pipelining process helps to speed up the processor and discuss the hazards that have to be taken care of in a pipe-lined processor?

OR

10 Why the directory cache coherence protocols are more scalable than snooping cache coherence protocols to achieve the performance?

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