Code: 9F00203

MCA II Semester Regular & Supplementary Examinations May 2016

COMPUTER ORGANIZATION

(For students admitted in 2010, 2011, 2012, 2013, 2014 & 2015 only)

Time: 3 hours Max. Marks: 60

Answer any FIVE questions

All questions carry equal marks

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1 (a) Simplify the following Boolean functions using four variable maps (K-maps):
$F(w, x, y, z) = \Sigma(0, 2, 4, 5, 6, 7, 8, 10, 13, 15)$

(b) Convert the hexadecimal number F4EAD5 to binary and Octal.

2 (a) Describe the memory connection (RAM and ROM chips) to CPU with suitable circuit diagram.

(b) Explain four-way set associative mapping technique for cache memory.

3 (a) Demonstrate the general configuration of a micro-programmed control unit.

(b) Give the micro-instruction code format (20 bits) and discuss symbols and binary code for microinstruction fields.

4 (a) With suitable examples, explain register indirect and index addressing modes.

(b) Give the list of registers and their function for the basic computer.

5 (a) How are assembler directives handled and executed? Give illustrations.

(b) Differentiate between arithmetic and logical shift operations.

6 (a) Discuss the strobe control method of asynchronous data transfer.

(b) Give a block diagram and explain daisy chain priority arrangement.

7 (a) Illustrate the behavior of a pipeline with a space time diagram.

(b) Describe briefly vector operations.

8 (a) Explain the working of a 5D hypercube network with a neat sketch.

(b) Suggest solutions to the cache coherence problem in multiprocessors.

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