Code: 9F00203

MCA II Semester Regular & Supplementary Examinations August 2014

COMPUTER ORGANIZATION

(For students admitted in 2009, 2010, 2011, 2012 & 2013 only)

Time: 3 hours Max. Marks: 60

Answer any FIVE questions
All questions carry equal marks
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1. (a) Draw the block diagram of a clocked synchronous sequential circuit and explain.
   (b) Design a 2 bit count-down counter. This is a sequential circuit with two flip-flops and one input x. When x = 0, the state of the flip-flops does not change. When x = 1, the state sequence is 11, 10, 01, 00, 11 and repeat.

2. (a) Describe in words and by means of a block diagram how multiple matched words can be read out from an associate memory.
   (b) Explain the concept of multiprogramming.

3. (a) What is the difference between a microprocessor and a micro program? Is it possible to design a microprocessor without a micro program? Are all micro programmed computers also microprocessors?
   (b) Show how a 9-bit micro operation field in a microinstruction can be divided into subfields to specify 46 micro operations. How many micro operations can be specified in one micro instruction?

4. (a) Explain about the field of an instruction format.
   (b) Explain about direct and indirect addressing modes.

5. Explain about the various types of unconditional JUMP instruction.

6. (a) List four peripheral devices that produce an acceptable output for a person to understand.
   (b) What is the basic advantage of using interrupt-initiated data transfer over transfer under program control without an interrupt?

7. (a) A non-pipeline system takes 50 ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10 ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speed up that can be achieved?
   (b) Explain four possible hardware schemes that can be used in an instruction pipeline in order to minimize the performance degradation caused by instruction branching.

8. (a) How many switch points are there in a crossbar switch network that connects p processors to M memory modules?
   (b) Discuss the difference between tightly coupled multiprocessors and loosely coupled multiprocessors from the viewpoint of hardware organization and programming techniques.

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