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## B. Tech **SEM III THEORY EXAMINATION 2017-18** DIGITAL LOGIC DESIGN

Time -3.00 hr Total Marks: 70

**Note: 1.** Attempt all sections. If require any missing data; then choose suitably.

#### SECTION - A

## 1. Attempt all questions in brief.

 $2 \times 7 = 14$ 

- (a) Write four advantages of Digital Systems over Analog Systems.
- (b) Write the Excitation table and characteristic equation of JK flip flop
- (c) Write the difference between combinational and sequential circuits.
- (d) What is  $(33)_6 + (45)_6$
- (e) Implement the Expression Y = ABC' + BD + E using Nand gate only.
- **(f)** Convert the following
  - (i)  $(562.13)_7 = (?)_{10}$
  - (ii)  $(467.342)_8 = (?)_{10}$
- (g) What is race around condition?

#### 2. Attempt any three of the following:

 $7 \times 3 = 21$ 

- (a) Simplify the following Boolean function using K-map Y = m(0,1,3,5,6,7,9,11,16,18,19,20,21,22,24,26)
- (b) Write the steps for combinational circuit designing and design a circuit of three input which gives an high output whenever the sum of LSB & MSB bit is 1.
- (c) Implement the function F = m(0,1,3,4,7,8,9,11,14,15) using 8:1 mux
- (d) Draw and explain the PISO, PIPO register.
- (e) Draw and explain 4-bit by 3-bit multiplier

#### SECTION - C

## 3. Attempt any one part of the following:

 $7 \times 1 = 7$ 

- (a) Design a universal shift register that performs HOLD, SHIFT RIGHT, SHIFT LEFT, & **LOAD**
- (b) Generate the hamming code for the word 11011. Assume that a single error occurs while storing the generated hamming code. Explain how this single error is detected.

#### 4. Attempt any one part of the following:

 $7 \times 1 = 7$ 

- (a) Draw and explain 4-bit magnitude comparator
- **(b)** Draw a decimal adder to add BCD numbers.

#### 5. Attempt any one part of the following:

 $7 \times 1 = 7$ 

(a) Draw and explain the operation of a RTL NOR gate

(b) Draw and explain the operation was a First Ranker green

### 6. Attempt any one part of the following:

 $7 \times 1 = 7$ 

(a) An asynchronous sequential logic circuit is described by the following excitation and output function

$$y=X_1X_2+(X_1+X_2)Y$$
 $Z=y$ 

Draw the logic diagram of the circuit, Also derive the transition table and output map.

(b) Design a 3 bit up/down ripple counter

## 7. Attempt any one part of the following:

 $7 \times 1 = 7$ 

- (a) Write short notes on RAM and PLA
- (b) Derive the state table and state diagram of the synchronous sequential circuit shown below (X is an input to the circuit). Explain the circuit function.

