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B. TECH.

THEORY EXAMINATION (SEM–IV) 2016-17

ELECTRONIC CIRCUITS

Time : 3 Hours *Max. Marks : 100*

Note : *Be precise in your answer. In case of numerical problem assume data wherever not provided.*

SECTION – A

1. Attempt all of the following questions: 10 x 2 = 20

(a) The input signal v_i to an op-amp is $v_i = 0.03 \sin 1.5x\ 10^5\ t$. What can be the maximum gain of an op-amp with slew rate of 0.4 volts/μs.

(b) Draw the circuit diagram of an integrator and find its output.

(c) What do you mean by slew rate and CMRR of an op-amp.

(d) Draw Hybrid –π model and T-model equivalent of NPN transistor.

(e) Explain Bakhausen criterion.

(f) What are the conditions for operation in triode and saturation region of NMOS and PMOS transistors?

(g) An amplifier has a mid-band gain of 125 and bandwidth of 250 KHz. If 4% negative feedback is introduced, find the new bandwidth and gain, also find the feedback ratio when the bandwidth is restricted to 1MHz.

(h) Draw the circuit of colpitts oscillator and also write its frequency and condition of maintaining oscillations.

(i) What is the principle of crystal oscillator?

(j) What are the internal capacitances of BJT?

SECTION – B

2. Attempt any five of the following questions: 5 x 10 = 50

(a) Explain inverting amplifier and also derive an expression for the closed loop gain under the assumption that the open loop gain is finite.

(b) Do the analysis of series-series feedback amplifier to derive gain, input resistance and output resistance.

(c) Draw the circuit of an RC phase shift oscillator using op-amp and derive frequency and condition of oscillation for RC phase shift oscillator.

(d) (i) Explain Hartley oscillator.

(ii) Differentiate between DMOSFET and EMOSFET.

(e) Do the analysis bias dc biasing circuit of the NPN transistor to derive Q point and of self stability factor.

(f) DO the small signal analysis of MOS differential pair to determine differential and common mode gain.

(g) (i) An enhancement type NMOS transistor with V_t =0.7 V has its source terminal grounded and a 1.5 V applied to the gate. In what region does the device operate for a) $V_D = 0.5$ v b) $V_D = 0.9$ v c) $V_D = 3$ v.

(ii) Explain the construction and working of N type enhancement MOSFET.

(h) (i) Draw input and output characteristics of common emitter amplifier.

(ii) State the properties of an ideal op-amp.

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SECTION – C

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Attempt any two parts of the following questions: **2 x 15 = 30**

3 Do the small signal analysis of common emitter amplifier with emitter resistance do derive input resistance, voltage gain (from base to collector), overall voltage gain (source to load), open circuit voltage gain and output resistance.

4 Explain the effect of finite loop gain and bandwidth on circuit performance. Also define input offset voltage and input offset current.

5 (i) Explain all four feedback topologies with their block diagram.

(ii) Explain the operation of LC tank circuit.

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