ldresses (in decimal) that will cause
CPU.
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RAM, 01 for ROM, and 10 for

AM and ROM chips are needed?
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ons. [2×10=20]
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Explain.

Printed Pages : 4

ECS-401

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 110405

Roll No.

B. Tech.

(SEM. IV) THEORY EXAMINATION, 2014-15

COMPUTER ORGANIZATION

Time : **3** Hours] [Total Marks : **100**

Note: (1) Attempt all question.
(2) All question carry equal marks.

1 Attempt any FOUR questions. [4×5=20]

(a) Given the 8 bit data word 10110100, generate the 13 bit composite word for the hamming code that corrects single errors and detects double errors.

(b) What do you mean by high speed adder ? Discuss design of high speed adders.

(c) What is the radix of the numbers if the solution to the quadratic equation $x^2-10x+31=0$ is x=5 and x=8 ?

(d) Represent decimal number 8620 in (a) BCD; (b) excess-3 code; (c) 2421 code; (d) as a binary number.

(e) Design an arithmetic circuit with one variable S and two-n bit data inputs A and B. The circuits generate the following four arithmetic operations in conjunction with the input carry C_{in}. Draw the logic diagram for the first two stages.

S	$C_{in} = 0$	$C_{in=1}$
0	$D = A + B(add)$	$D = A + 1(increment)$
1	$D = A - 1(decrement)$	$D = A + B' + 1(subtract)$

(f) What do you mean by Bus and explain bus interconnection ?

Attempt any FOUR questions. [4×5=20]

(a) What are addressing modes? What is the need of having many addressing modes in your machine? Discuss indirect and register indirect addressing in details.

(b) What is an array multiplier? Design an array multiplier that multiplies two 4-bit numbers. Use AND gates and binary adders.

(c) What is ROM? How does PROM differ form EEPROM.

(d) What is Stack Organization ? Compare register stack and memory stack ?

(e) Specify the control word that must be applied to the processor to implement the following micro-operation.

(1) R1 ← R2+R3

(2) R4 ← R4

(3) R5 ← R5-1

(4) R6 ← shl R1

(5) R7 ← input

(f) Draw the hardware details for Booth Multiplication algorithm and using Booth's Multiplication method multiply decimal number (-23) and (+9).

3 Attempt any TWO questions. [2×10=20]

(a) Explain the difference between hardwired control and micro programmed control. Is possible to have a hardwired control associated with a control memory?

(b) What is the meaning of the term one-address instruction ? How can an instruction, which requires three operands be executed in such machine ? Explain with the help of an example.

(c) Write a program to evaluate the arithmetic statement:

$$X = \frac{A - B + C * (D * E - F)}{G + H * K}$$

(1) Using an accumulator type computer with one address instruction.

(2) Using a stack organized computer with zero address operation instructions.

4 Attempt any TWO question. [2×10=20]

1 (a) Explain LIFO, FIFO and CPU page replacement algorithm with example.

(b) A virtual memory has a page size of 1K words. There are eight pages and four blocks.

The associative memory page table contains the following entries.

Page	*Block*
0	3
1	1
4	2
6	0

Make a list of all virtual addresses (in decimal) that will cause a page fault if used by CPU.

2 A Computer employs RAM chips of 256 × 8 and ROM chips 1024×8. The computer system needs 2K bytes of RAM, 4K bytes of ROM and 4 interface units, each with four registers. A memory mapped I/O configuration is used. The Two highest-order bits of the address bus are assigned 00 for RAM, 01 for ROM, and 10 for interface registers.

(a) How many RAM and ROM chips are needed?

(b) Draw a memory address map for the system.

(c) Give the address range in hexadecimal for RAM, ROM and interface

3 What do you mean by memory management hardware? Explain the basic components of memory management unit.

5 Attempt any TWO questions. [2×10=20]

(a) Describe asynchronous date transfer. What are the methods through which it can be achieved? Explain Stroke control and Handshaking.

(b) What are the various standard communication interfaces? Explain with the help of synchronous communication?

(c) Describe DMA with suitable block diagram, Why does DMA have priority over the CPU when both request a memory transfer? Explain.

Printed Pages : 4

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PAPER ID : 110405

Roll No.

(SEM. IV) THEOR

COMPUTE

Time : **3** Hours]

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(e) Design an arithr n bit data inpu following four the input carry two stages.