Printed Pages : 4 | 387 | NEC-501

(Following Paper ID and Roll No. to be filled in your Answer Book)

Paper ID : 131501 Roll No. | | | | | | | | | | |

B.Tech

(SEM. V) (ODD SEM)

THEORY EXAMINATION , 2015-16

INTEGRATED CIRCUITS

Time:3 hours] **[MaximumMarks:100**

Section-A

1. Attempt all parts. All parts carry equal marks. Write answer of each part in short. **(2x10=20)**

   (a) Why don't we normally realize the beta-compensated current mirror using MOS?

   (b) What are the basic blocks of phase-locked loop?

   (c) What do you understand by hysteresis voltage?

   (d) What is the role of coupling capacitor (C_c) in IC 741 internal circuit?

   (e) Give the example of a square wave generator which utilizes positive feedback.

   (f) What is capture range in PLL?

(g) What is the chip number for phase locked loop?

(h) Define the term V_{IH} and V_{IL} for the CMOS inverter.

(i) The basic step of 9 bit DAC is 10.3mV. if 000000000 represents 0 V, what output is produced if the input is 101101111?

(j) Define noise margin for the CMOS inverter.

Section-B

Note: Attempt any five questions from this section.

(10x5=50)

2. What do you understand by the base current compensated current mirror? How does it provide improvement over simple current mirror circuit? Expalin with the help of a neat circuit diagram.

3. Define the slew rate. Also derive the relationship between f_t and slew rate for the IC 741.

4. Sketch the properly labeled Master Slave D flip-flop circuit and explain its operation with the help of proper waveform of the clock signal.

5. What is a DAC? Describe the weighted resistor DAC. Give mathematical expressions in support of your answer.

6. Determine Ic_1, Ic_2, Ic_3 for the circuit shown in figure 1. Assume $\beta = 125$.

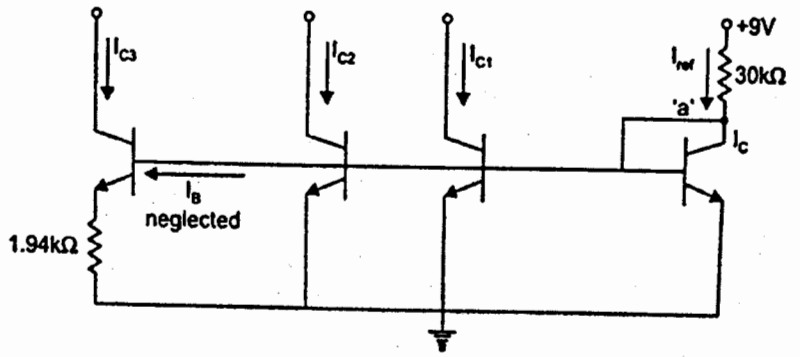

Figure 1

7. Draw the functional block diagram of IC 555 and explain its working. Design a 555 timer as an Astabel multivibrator with an output signal timer frequency of 700 Hz and 60% duty cycle.

8. Describe the Antoniou inductance simulation circuit with properly labelled circuit diagram and give mathematical expressions in support of your answer.

9. Describe the sample and hold circuit with the help of an op-amp. What are the applications of sample and hold circuit?

Section-C

Note: Attempt any two questions from this section.

(15x2=30)

10. Describe the circuit for the KHN filter using three op-amp. Design a second order butterworth low-pass filter having upper cut-off frequency 1kHz. Determine its frequency response.

11. Describe different regions of operation for CMOS inverter over its VTC characteristics.

    Consider a CMOS inverter with following parametrs :

    $V_{DD} = 3.3$ V, $V_{T0,n} = 0.6$V, $V_{T0,p} = 0.7$V, $K_n = 200\,\mu$A/V^2, $K_p = 80\,\mu$A/V^2

    Calculate the noise margin of the CMOS inverter circuit.

12. Describe the Schmitt trigger with the help of proper circuit diagram and transfer characteristics. A Schmitt trigger with the upper threshold level $V_{UT} = 0$V and hysteresis width is 0.2V converts 1kHz sine wave of amplitude $4V_{pp}$ into a square wave. Calculate the time duration of the negative and positive portion of the output waveform.

—x—