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Sub Code: NEC501

Paper Id:3049

Roll No:

**B TECH**  
**(SEM 5) THEORY EXAMINATION 2017-18**  
**INTEGRATED CIRCUITS**

Time: 3 Hours

Total Marks: 100

Notes:

**Note :-** All sections are compulsory.If require any missing data; then choose suitably.

**SECTION – A**

- 1** This question consist of short answer questions. Attempt **all parts** of this question. All parts carry equal marks.

**2 X 10 = 20**

- a) If the open loop gain of an operational amplifier is very large. Does the closed loop gain depend upon the external components or the operational amplifier justify
- b) What is meant by the term matched transistors.
- c) Define and give significance of Slew Rate.
- d) What is a Super Diode.
- e) Give two application of analog multiplier.
- f) What do you mean by a frequency response of a filter circuit.
- g) Differentiate between Comparator and Schmitt trigger.
- h) Describe the need of voltage limiter circuits.
- i) The basic step of a 8-bit DAC is 20mV. If 00000000 represents 0V, what is represented by the input 10110111.
- j) What do you mean by a CMOS circuit logic.

**SECTION – B**

- 2** Attempt **any Three** parts of this question. All parts carry equal marks.

**10 X 3= 30**

- (a) What are the desirable characteristics of current mirror circuits. Explain the circuit of Wilson MOS current mirror. Also discuss how it can be improved.
- (b) Derive the expression of voltage gain in KHN Biquad Filter. Draw the KHN Biquad filter and drive transfer function of the BPF and LPF from that.
- (c) Discuss the features of CMOS circuit. Realize one AND-OR-INVERT (AOI) and one OR- AND-INVERT (OAI) function using CMOS logic circuit.
- (d) What do you mean by the quadrant operation of multiplier. Draw and explain a GILBERT analog multiplier.



- (e) Draw the block diagram of a PLL and explain its operation. Explain lock-in-range, capture range and pull-in time of a PLL. List the application of PLL.

### SECTION – C

Attempt **any Two parts** of each questions of this section. All question carry equal marks

**10 X 5 = 50**

3.
  - a) Describe the operation and characteristics of a BJT complementary push-pull output stage.
  - b) Determine the small-signal model of the second stage of the 741 op-amp.
  - c) The parameter of the three transistor CM are  $V_{CC} = 9V$ ,  $V_{EE} = 0$ ,  $R_1 = 12K\Omega$ ,  $V_{BE(on)} = 0.7V$ ,  $\beta = 75$ ,  $V_A = \infty$ . Calculate the value of current,  $I_{ref}$ ,  $I_o$ ,  $I_{C1}$ ,  $I_{B1}$ ,  $I_{B2}$ ,  $I_{B3}$ ,  $I_{E3}$ .
4.
  - a) Draw the generalized impedance converter and derive its impedance equation. Also simulate an Inductor.
  - b) Derive the output expression for RC Phase Shift Oscillator.
  - c) Compare and contrast active filters and passive filters. Design a second order low pass Butterworth filter to have cut-off frequency of 1KHz.
5.
  - a) Give CMOS implementation of a SR flip-flop and explain its working.
  - b) Give two different CMOS realization of the Exclusive – OR gate function in which the PDN and PUN are dual networks..
  - c) Discuss D-F/F circuit using NAND CMOS gates.
6.
  - a) Draw & explain the circuit of triangular wave generator. How square wave can be obtained using this triangle wave.
  - b) Describe temperature compensated Log amplifier using two op-amp & explain its operation.
  - c) Explain how a Schmitt Trigger circuit works with a neat diagram. Design an Schmitt trigger with  $V_{UT} = 2V$ ,  $V_{LT} = -1V$ . Assume  $\pm V_{sat} = \pm 13V$ .
7.
  - a) Draw and Explain the block diagram of IC 555.
  - b) Explain the operation of dual slope ADC.
  - c) Design a 555 timer as astable multivibrator giving its block diagram which provide an output signal frequency of 2 KHz and 75 % duty cycle.