Printed Pages: 3 NEC-703

(Following Paper ID and Roll No. to be filled in your Answer Books)

Paper ID : 2012358 Roll No.

B.TECH.

Regular Theory Examination (Odd Sem-VII), 2016-17

VLSI DESIGN

Time : 3 Hours *Max. Marks : 100*

SECTION - A

1 **Attempt all questions. All parts carry equal marks. Write answer of each part in short.** **(10×2=20)**

a) What do you meant by threshold voltage of MOS transistor? Explain

b) List the steps used for CMOS fabrication.

c) Define delay time and discuss delay models.

d) Name any two basic CAD tools and explain.

e) Describe basic principle of pass transistor circuits.

f) Write the importance low power in VLSI architectures.

g) Bring out the drawbacks of dynamic logic.

h) Distinguish between SRAM and DRAM.

i) Classify adiabatic logic circuits.

j) Mention the scaling principles. What is the need for scaling.

SECTION - B

Note: Attempt any five questions from this section. (5×10=50)

2. Analyze the characteristics of CMOS inverter with neat sketch.
3. What do you mean by Design for testability. Discuss scan based techniques.
4. Narrate in detail about VLSI low power architectures with suitable diagram.
5. Design an 8MB X 16 bit memory architecture using 512K X 8 bit memory chip.
6. Explain the Ad Hoc testable design techniques with a suitable example.
7. Illuminate the n-well CMOS fabrication process with neat diagrams.
8. Analyze the different gate delay model of CMOS gate transistor.
9. Differentiate between EEPROM and Flash memory.

SECTION - C

Note: Attempt any two questions from this section. (2×15=30)

10. Implement a 2 input NAND gate using:
    a) Dynamic CMOS logic

b) Domino CMOS logic

11. Derive the expression for total power dissipation of a CMOS circuit.
12. Narrate in detail about the operation of NMOS transistor with different operating modes.