Printed Pages : 1 Roll No. EEC032

B.TECH.

THEORY EXAMINATION (SEM–VIII) 2016-17

DIGITAL SYSTEMS USING VHDL

Time : 3 Hours ***Max. Marks : 100***

Note : *Be precise in your answer. In case of numerical problem assume data wherever not provided.*

SECTION – A

1. Explain the following: **10 x 2 = 20**

(a) Differentiate between Combinational and Sequential Circuits.

(b) Write Application and Advantages of VHDL

(c) Write VHDL code for Full Adder using structural style of modelling.

(d) What are Generic parameters?

(e) Write VHDL code for 4:2 encoder using Behavioural style of modelling.

(f) What are different levels of abstractions of digital design?

(g) Define Lexical elements, signals and Variable.

(h) What is inertial delay?

(i) Write the VHDL code for 2:4 MUX in structural style

(j) What are binding alternatives?

SECTION – B

2. Attempt any five parts of the following questions: **5 x 10 = 50**

(a) Explain Delta delay and transaction appending rules.

(b) Discuss Sequential modelling and attributes.

(c) What is basic structure of VHDL? Write the VHDL code for 4:16 multiplexer.

(d) Write VHDL code for 16 bit SIPO Shift register.

(e) What are synthesis rules and styles for hardware core and models?

(f) Write VHDL code for D Flip Flop.

(g) What is Guarded signal Assignment? Explain with example.

(h) Explain inertial and transport delay mechanism with comparison.

SECTION – C

Attempt any two parts of the following questions: **2 x 15 = 30**

3 Explain Testing and its different issues related to design test

4 Write the behavioural VHDL code for RAM.

5 Explain logic behind floating point multiplication.