

Code: 9D06103

M.Tech I Semester Supplementary Examinations August 2016

ADVANCED COMPUTER ARCHITECTURE

(Common to DSCE, DECS & ES)

(For students admitted in 2012, 2013, 2014 & 2015 only)

Time: 3 hours

Max. Marks: 60

Answer any FIVE questions
All questions carry equal marks

- 1 (a) Write about reporting, performance quantitative principles of computer design.
(b) Briefly explain about cost measuring principles in computer design.
- 2 (a) Write about addressing modes for signal processing.
(b) Write short notes on operations in the instruction set.
- 3 (a) Write the limitations of ILP with a special mention on realizable processors.
(b) What is branch prediction? Explain the various schemes in detail.
- 4 Explain the need for hardware support for exposing more parallelism at compile time.
- 5 (a) Briefly explain about performance of a cache.
(b) How cache behavior can be improved by reducing the miss rate? Explain it.
- 6 Explain in detail the symmetric shared memory architectures with reference to multiprocessor cache coherence problem.
- 7 Explain the bus standards and the interfaces. With timing diagrams, explain the read and write operations occurring in a typical bus.
- 8 Write about practical issues in interconnecting networks.
