Code: 17D06101

M.Tech I Semester Regular & Supplementary Examinations January/February 2019

STRUCTURAL DIGITAL SYSTEM DESIGN

(Common to DECS, ECE, DSCE, ES, VLSI&ES, ES&VLSI, VLSI&ESD, VLSI, VLSIS and VLSISD)

(For students admitted in 2017 & 2018 only)

Time: 3 hours Max. Marks: 60

Answer all the questions

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1 (a) Implement the following Boolean function using 8:1 multiplexer.
$F(A, B, C, D) = \Sigma m(1, 2, 4, 6, 7, 11, 13, 15)$

(b) What is the need of ALU and explain about it?

OR

2 Construct a 5 to 32 line decoder with four 3 to 8 line decoders with enable and a 2 to 4 line decoder.

3 (a) Explain top-down design methodology with example.

(b) Discuss about the separation of controller and architecture.

OR

4 What are the basic elements of ASM chart explain clearly with an example?

5 Briefly explain about multiplexer controller method and one shot method.

OR

6 Briefly discuss about fault diagnosis and testing with flow diagram.

7 Discuss about the 2910 micro program sequencer.

OR

8 Explain about design of micro programmed minicomputer.

9 Write short notes on simulators and schematic entry.

OR

10 Design a system for serial to parallel data conversion.

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