Code: 17D06103

M.Tech I Semester Regular & Supplementary Examinations January/February 2019

ADVANCED COMPUTER ARCHITECTURE

(Common to DSCE, ES, VLSI&ES, ES&VLSI, VLSI&ESD, VLSI, VLSIS and VLSISD)

(For students admitted in 2017 & 2018 only)

Time: 3 hours Max. Marks: 60

Answer all the questions

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1 Explain three shared memory multiprocessor models in detail.

OR

2 Explain with diagrammatic illustration Flynn's classification.

3 How can we partition a program into parallel branches, program modules, micro tasks or grains to yield the shortest possible execution time? What is the optimal size of concurrent grains in a computation?

OR

4 What is meant by interconnection structure? Mention various types of interconnection structures.

5 Explain the architecture of a Very Long Instruction Word (VLIW) processor and its pipeline operation.

OR

6 Describe the virtual addressed split cache design in Intel i860 with suitable example.

7 Explain the different stages of instruction pipeline design with neat diagrammatic presentation.

OR

8 In addition to streamline connection, nonlinear pipeline support feed forward and feedback connections. Explain them in detail with reservation and latency analysis.

9 What do you meant by cache coherence problem? Describe various protocols for cache coherence.

OR

10 Define deadlock. Explain how deadlock can be avoided in message passing mechanism.

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