Code: 17D06202

M.Tech I Semester Regular & Supplementary Examinations January/February 2019

CPLD & FPGA ARCHITECTURES & APPLICATIONS

(Common to ES, VLSI&ES, ES&VLSI, VLSI&ESD, VLSI, VLSI and VLSISD)

(For students admitted in 2017 & 2018 only)

Time: 3 hours Max. Marks: 60

Answer all the questions

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1 (a) With neat block diagram, explain the architecture of Xilinx Cool Runner XCR3064XL CPLD.
(b) When is CPLD better suited than SPLD? List out the comparisons between those two.

OR

2 (a) Draw the basic block diagram of PLA device and explain each block. List out its applications.
(b) Implement the following combinational circuit Boolean function:
$F_1(A,B,C)=\sum(0,1,2,4)$
$F_2(A,B,C)=\sum(0,5,6,7)$ using PLA.

3 (a) How does the architecture of a typical FPGA device differ from that of a CPLD? In what way does the architecture affect the timing performance in the two cases?
(b) Describe the technology mapping for FPGA.

OR

4 (a) Explain the concept of meta stability and when does meta stability cause design failures.
(b) Discuss following FPGA classification on user programmable switch technologies:
(i) SRAM. (ii) Anti-fuse. (iii) EEPROM.
And discuss the trade off.

5 Draw the logic diagram of Xilinx 4000 CLB and I/O blocks and explain their function.

OR

6 (a) Implemented simple and Fast-Ripple-Carry Counter Built with One Bit per CLB in the XC3000.
(b) Discuss the design Trade-Offs in SRAM-programmable FPGA Architecture.

7 (a) Compare the performance parameters of ACTEL based FPGAs ACT-1, 2 and 3.
(b) Explain about different programmable elements in FPGA architectures.

OR

8 (a) How the ACT-3 architecture is different from ACT-2 architecture? Explain the ACT-3 architecture in detail.
(b) Explain the ACT-2 architecture for high fan-in example.

9 (a) Explain state machine design for a 4-channel DMA controller.
(b) List criteria that influence performance of logic in FPGA designs.

OR

10 (a) Discuss chip level design considerations for ACT-1 and ACT-2 FPGA design.
(b) Explain high-performance loadable six-bit counter using pre-scaled counter design.

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