Code: 9D06106b

M.Tech I Semester Regular & Supplementary Examinations February 2016

DSP PROCESSORS & ARCHITECTURES

(Common to DSCE, DECS & ECE)

(For students admitted in 2011, 2012, 2013, 2014 & 2015 only)

Time: 3 hours Max Marks: 60

Answer any FIVE questions

All questions carry equal marks

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1 (a) What are the different types of digital filters? Explain in detail about them with necessary examples.
(b) Explain about decimation and interpolation with examples.

2 (a) What are the sources of errors in DSP implementation? Explain in brief.
(b) What is dynamic range and precision? What are the different number formats for signals and coefficients in DSP system?

3 (a) Draw and explain with neat diagrams bus architecture and memory of DSP processor.
(b) Explain about data addressing capabilities and address generation unit.

4 (a) What is an interrupt? Explain about interrupt effects.
(b) What is pipeline depth? Explain about its performance.

5 (a) Explain about data addressing modes of TMS320C54XX processor.
(b) Explain about interrupts of TMS320C54XX.

6 (a) What is an interpolation filter? Explain the implementation of digital interpolation using FIR filter and poly phase sub filter.
(b) Explain with the help of a block diagram and mathematical equations about the implementation of a second order IIR filter.

7 (a) What do you mean by bit-reversed index generation and how it is implemented in TMS320C54XX DSP assembly language?
(b) Derive the equation to implement a butterfly structure in DITFFT algorithm.

8 (a) Explain about memory interface with timing diagram.
(b) Explain about programmed I/O interface with flow chart and its read write sequence operations with neat sketches.

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