Code: 9D06106b

M.Tech I Semester Regular & Supplementary Examinations January/February 2017

DSP PROCESSORS & ARCHITECTURES

(Common to DSCE, DECS & ECE)

Time: 3 hours Max. Marks: 60

Answer any FIVE questions

All questions carry equal marks

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1 For the FIR filter Y[n] = [x(n) + x(n-1) + x(n-2)]/3. Determine:
   (a) System response function.
   (b) Phase response function.
   (c) Magnitude response function.

2 (a) Write notes on A/D conversion errors.
   (b) Find the decimal equivalent of the floating point number 1011000011100. Assume a format similar to IEEE-754 in which the MSB in the sign bit followed by 4 exponent bits followed by 8 bits followed by 8 bits for the fractional part.

3 (a) Design a 4X4 barrel shifter with neat diagrams.
   (b) Explain in detail about on chip memory.

4 (a) Explain the concept of pipelining with various stages with an example.
   (b) Explain about interlocking.

5 (a) Explain the interrupts of TMS 320C54XX processors.
   (b) Explain in detail about on chip peripherals.

6 (a) Write notes on adaptive filters.
   (b) Represent each of the following as 16 bit numbers in the desired Q-notation.
      (i) 0.3125 as Q_{15} number.
      (ii) -0.3125 as a Q_{15} number.

7 Determine the following for a 128 point FFT computation:
   (a) Number of stages.
   (b) Number of butterflies needed for the entire computation.
   (c) Number of butterflies that require real twiddle factors.

8 How does DMA helps in increasing the processing speed of a DSP processor?

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