



**Code: 9D06106c**

M.Tech I Semester Regular & Supplementary Examinations January/February 2017

**LOW POWER VLSI DESIGN**

(Common to DSCE & DECS)

Time: 3 hours

Max. Marks: 60

Answer any FIVE questions  
All questions carry equal marks

\*\*\*\*\*

- 1 (a) What are the various aspects to be considered in low-power VLSI design? Explain.  
(b) What are the advantages and limitations of silicon-on-insulator technology?
- 2 (a) Explain the isolation requirements in Bi-CMOS process.  
(b) Describe the process for integrated/digital CMOS IC.
- 3 (a) Floating body effects may also cause the parasitic bipolar leakage current in CMOS-SOI pass gate transistor, explain?  
(b) What are the future trends in Bi-CMOS process? Explain.
- 4 (a) With the help of equations, describe the level 1 and level 2 models of MOSFET.  
(b) Discuss about MOSFET in a hybrid mode environment.
- 5 (a) How threshold voltage adjustments can be carried out for CMOS devices? Explain with the help of necessary equations.  
(b) Give the performance evaluation of merged Bi-CMOS logic gates. How the weak points of conventional Bi-CMOS logic gates are overcome by these circuits?
- 6 (a) Explain about the functionality theme and synchronous schemes of latches and flip-flops.  
(b) What are the performance measures of latches and flip flops?
- 7 (a) Discuss about CMOS floating node concept.  
(b) Describe low power techniques for SRAM.
- 8 (a) Explain about comparison of advanced Bi-CMOS digital circuits.  
(b) Discuss about ESD-free Bi-CMOS.

\*\*\*\*\*