Code: 9D06101

M.Tech I Semester Supplementary Examinations August/September 2018

DIGITAL SYSTEM DESIGN

(Common to DSCE, DECS, ECE, VLSIES, ESVLSI, VLSIESD & MNE)

(For students admitted in 2013, 2014, 2015 & 2016 only)

Time: 3 hours Max. Marks: 60

Answer any FIVE questions

All questions carry equal marks

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1 Develop an ASM chart to design control logic of a binary divider and realize the same.

2 (a) Design an iterative comparator circuit to compare two n bit numbers.
(b) How a sequential circuit can be designed using FPGA?

3 Explain about the following types of faults:
(a) Stuck at faults.
(b) Bridge faults.
(c) Temporary faults.

4 (a) Discuss in detail Boolean difference method in combinational circuits.
(b) What is the significance of Kohavi algorithm? Explain how it detects multiple faults in two-level-networks with a simple example.

5 Classify the fault detection experiments for the sequential circuits and explain.

6 Design a 3-bit BCD to grey code converter and realize the circuit using PLA and then show that how folding will reduce the number of cross points given on the PLA.

7 Explain in detail testable PLA design with an example.

8 The output Z of a fundamental-mode, two input sequential circuit is to change from 0 to 1 only when X_2 changes from 0 to 1 while $X_1 = 1$. The output is to change from 1 to 0 only when X_1 changes from 1 to 0 while $X_2 = 1$. (i) Find a minimum-row reduced flow table, the output should be fast and flicker-free. (ii) Show a valid assignment and write a set of (static) hazard-free excitation and output equations.

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