Code: 9D06106b

M.Tech I Semester Supplementary Examinations August/September 2018

DSP PROCESSORS & ARCHITECTURES

(Common to DSCE, DECS and ECE)

(For students admitted in 2013, 2014, 2015 & 2016 only)

Time: 3 hours Max. Marks: 60

Answer any FIVE questions

All questions carry equal marks

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1 (a) Draw and explain the block diagram of a digital signal-processing system.
(b) Write a matlab code to generate a square pulse.

2 (a) What are the different number formats that are used to represent signals and coefficients in DSP systems? Explain any two of them.
(b) Briefly analyse the different sources of error in DSP implementations.

3 (a) Differentiate the Von Neuman and Harvard architecture. Justify which architecture is best.
(b) Write short notes on the address generation unit of DSP devices.

4 (a) Write short notes on stack with its internal structure in a DSP.
(b) Explain the concept of pipelining for speeding up the execution of an instruction.

5 (a) Write short notes on the on chip hardware timer of TMS320C54XX.
(b) With a block diagram, explain the direct addressing mode of TMS320C54XX.

6 With an example, explain how 2D signal processing is implemented using a DSP processor.

7 Write an assembly language or C program using TMS320C54XX to bit reverse a 8 bit number and draw the flowchart.

8 (a) Write short notes on I/O interface and memory interface to a DSP.
(b) How are the channels differentiated in the multichannel buffered serial port interface?

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