Code: 9D06106c

M.Tech I Semester Supplementary Examinations August/September 2018

LOW POWER VLSI DESIGN

(Common to DSCE and DECS)

(For students admitted in 2013, 2014, 2015 & 2016 only)

Time: 3 hours Max. Marks: 60

Answer any FIVE questions

All questions carry equal marks

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1 (a) Compare low-power VLSI design techniques with conventional design methods.
(b) Explain about the design limitations imposed on low-power, low-voltage circuits pertaining to the following parameters: (i) Power supply voltage. (ii) Scaling.
(c) What are the advantages and limitations of silicon-on-insulator technology?

2 (a) Give the complete process flow for 0.2 µm in SOI Bi-CMOS process.
(b) Describe the process for integrated analog-digital CMOS I.C.

3 (a) Explain about narrow channel effects of SOI CMOS devices due to cross section and threshold voltage.
(b) What are the future trends in Bi CMOS process? Explain.

4 (a) Describe the advanced MOSFET models. What are the limitations of this model?
(b) Describe the temperature dependent hybrid model device threshold model of MOSFET.

5 (a) Discuss the characterization and power consumption of Bi-CMOS gates.
(b) With the help of a schematic diagram, explain about the working of an FS-M Bi CMOS logic gate.

6 (a) In what way relay logic circuits differ from pass transistor logic circuits. Why the output of a pass transistor circuit is not used as a control signal for the next stage?
(b) Explain with an example how pipelining and parallelism can be combined to realize low power circuits. To realize how power circuits.
(c) Realize and implement NAND / AND logic and XOR / XNOR logic using CPL logic.

7 (a) What are the quality measures for latches and flip-flops? Explain.
(b) Give the design perspective for edge triggered D-flip-flop.

8 (a) Explain the clock skew problem of dynamic CMOS circuits.
(b) Floating body effects may also cause the parasitic bipolar leakage current in CMOS-SOI pass gate transistor- Explain?
(c) Explain different pre-charge techniques employed by SRAM's.

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