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Code: 9D06101

M.Tech I Semester Supplementary Examinations February/March 2018 **DIGITAL SYSTEM DESIGN**

(Common to DSCE, DECS, ECE, VLSIES, ESVLSI, VLSIESD & MNE) (For students admitted in 2012, 2013, 2014, 2015 & 2016 only)

Time: 3 hours

Max. Marks: 60

Answer any FIVE questions All questions carry equal marks

- Draw an ASM chart to design a control logic of a binary multiplier. Realize the same using 1 MUX, decoder and D-type flip flops.
- 2 Design a sequential circuit to convert excess 3 to BCD code using PLA and D flip-flops.
- (a) Explain in detail the path-sensitization technique with an example. 3
 - (b) Define Kohavi algorithm. Explain this algorithm with an example.
- (a) Describe the algorithmic steps involved in PODEM with an example. 4
 - (b) Write a brief note on random testing.
- 5 Explain in detail about state identification and fault diagnosis in a sequential circuit.
- (a) Realize the following expression using PLA. 6
 - f = x'y'z + x'yz + xyz + xy'z' and explain PLA minimization.
 - (b) What is the need for PLA folding and describe in detail PLA folding with examples?

- IS a sl. Explain different types of fault models and fault types in a PLA. 7
- 8 Write a short note on:
 - (a) Minimal closed covers.
 - (b) Cycles and races.