Code: 9D06103

M.Tech I Semester Supplementary Examinations February/March 2018

ADVANCED COMPUTER ARCHITECTURE

(Common to DSCE, DECS & ES)

(For students admitted in 2012, 2013, 2014, 2015 & 2016 only)

Time: 3 hours Max. Marks: 60

Answer any FIVE questions

All questions carry equal marks

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1 (a) State and explain Amdahl's law.
(b) How to measure performance of a computer? Describe.

2 (a) List the major types of optimizations and then explain the same with examples.
(b) Describe with examples, the most common addressing modes.

3 (a) Draw and explain the basic structure of a MIPS floating point unit using Tomasulo's algorithm.
(b) What is a branch-prediction filter? Explain the states in a two-bit prediction scheme.

4 (a) Examine the use of compiler-based techniques for branch prediction.
(b) Describe in detail the basic VLIW approach.

5 Brief out the five cache miss penalty reduction techniques.

6 (a) What is meant by multithreading? Explain the two main approaches to multithreading.
(b) What is a barrier? Develop a code for: (i) Simple barrier. (ii) Sense-reversing barrier.

7 (a) Draw and explain a typical interface of I/O devices and an I/O bus to the CPU memory. Also explain the main options for design of a bus.
(b) Define the following: (i) Module reliability. (ii) Module availability.

8 (a) Describe in detail any one example of cluster design.
(b) Explain the following practical in interconnection networks:
(i) Connectivity. (ii) Standardization. (iii) Fault tolerance.

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