Code: 9D06106b

M.Tech I Semester Supplementary Examinations February/March 2018

DSP PROCESSORS & ARCHITECTURES

(Common to DSCE, DECS & ECE)

(For students admitted in 2012, 2013, 2014, 2015 & 2016 only)

Time: 3 hours Max. Marks: 60

Answer any FIVE questions

All questions carry equal marks

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1 (a) Differentiate decimation and interpolation.
(b) Write a matlab code to generate power spectrum of a sine wave.

2 (a) How can quantization error and overflow error be reduced?
(b) Discuss the analogue to digital conversion errors occurring in a DSP system.

3 (a) Design an interface to connect a 64k x 16 flash memory to a DSP processor.
(b) What are the blocks which differentiate a DSP processor and an ordinary microprocessor?

4 Design a pipelined FIR digital filter and justify the increase in speed.

5 (a) Draw the internal architecture of TMS320C54XX processor and explain each of its blocks.
(b) Discuss the data addressing modes of TMS320C54XX processor.

6 With a flow diagram, explain how an IIR filter is implemented using a DSP processor.

7 Write an assembly language or C program using TMS320C54XX to implement a 8-point FFT and draw the flowchart.

8 (a) Interface a DMA controller with a DSP processor.
(b) Give the I/O map.

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